

FIG. 1

FIG. 1 is a block diagram of a communication system 1000, in accordance with an embodiment of the present invention.

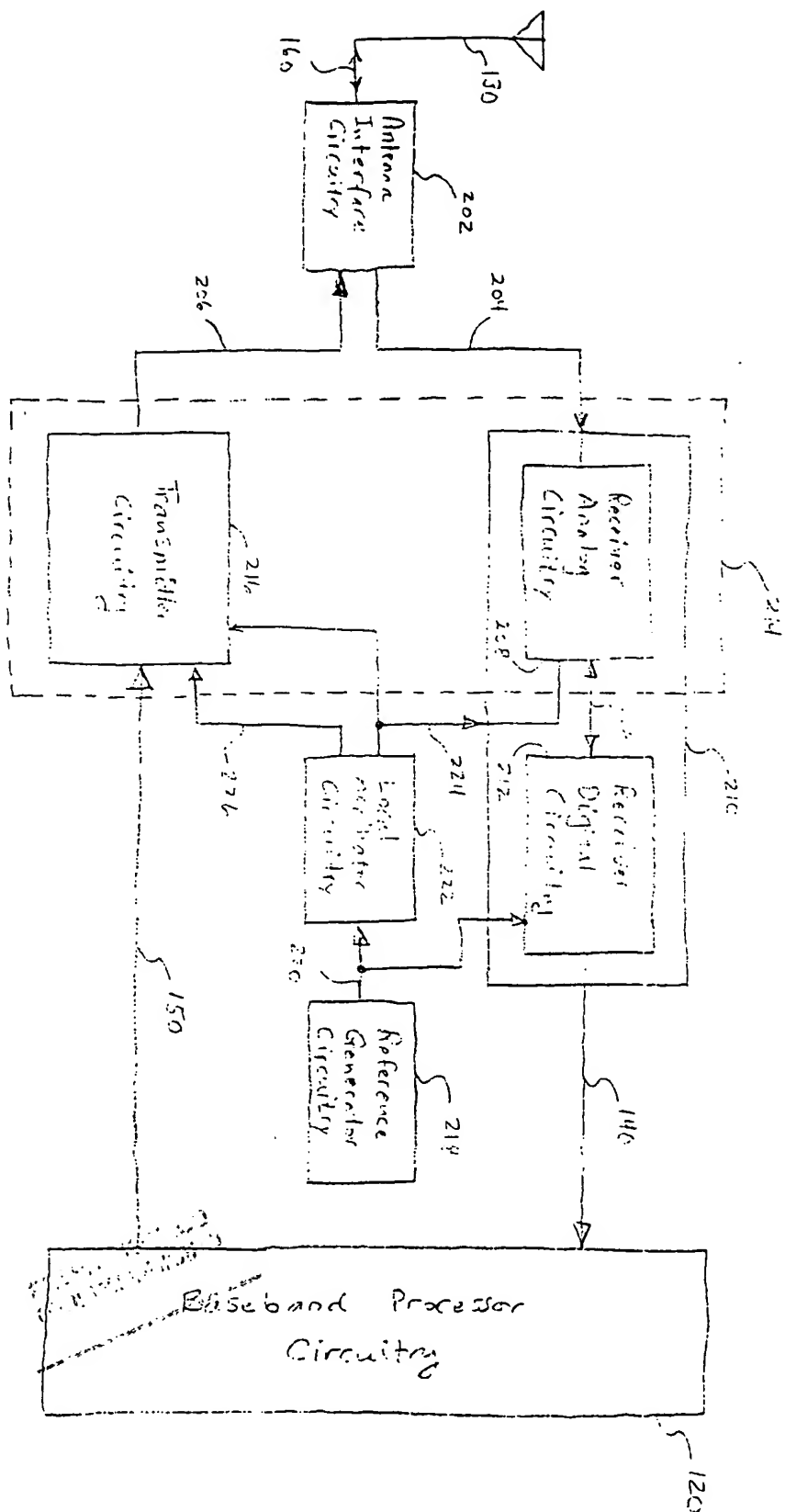


FIG. 2A

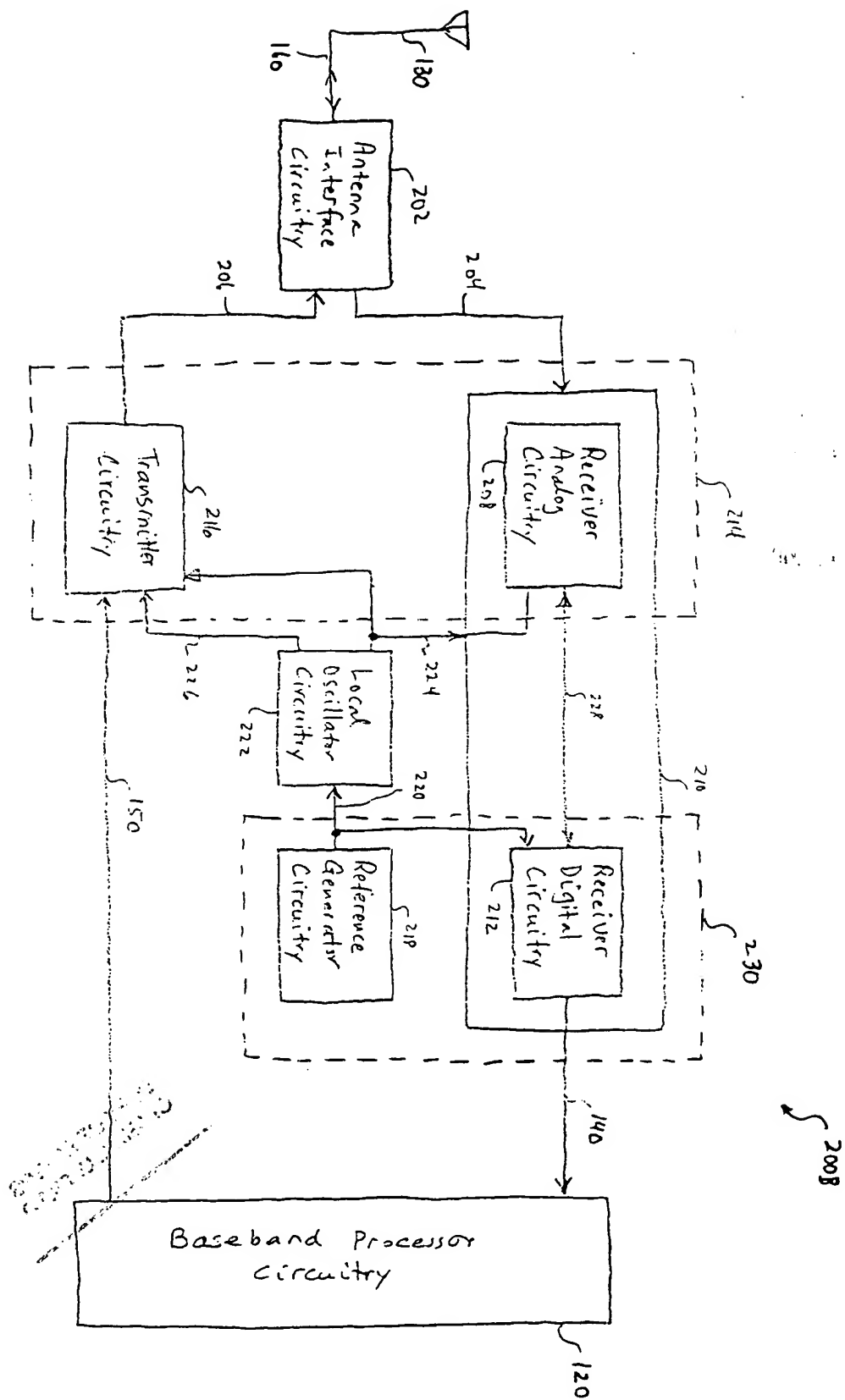


FIG. 2B

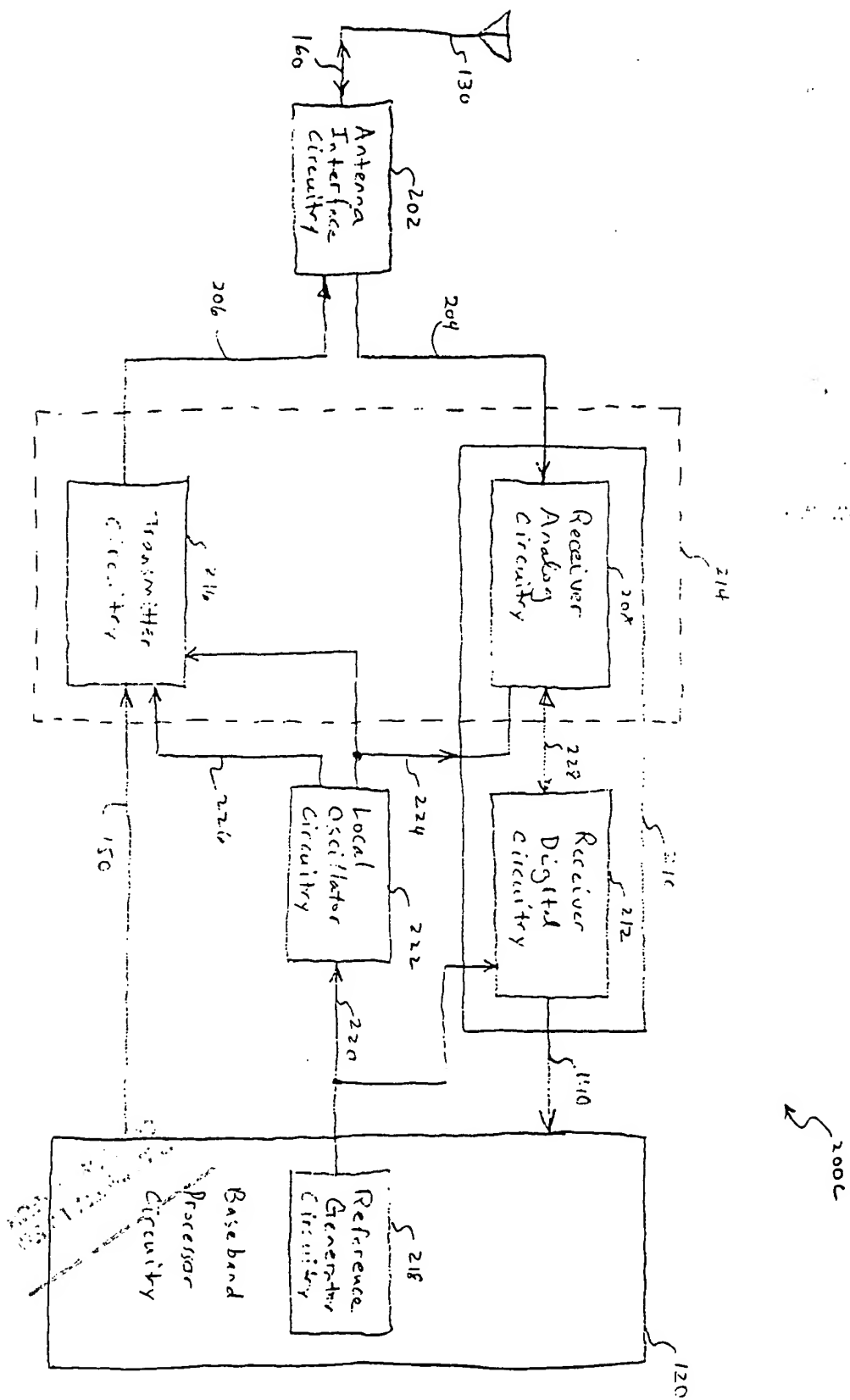
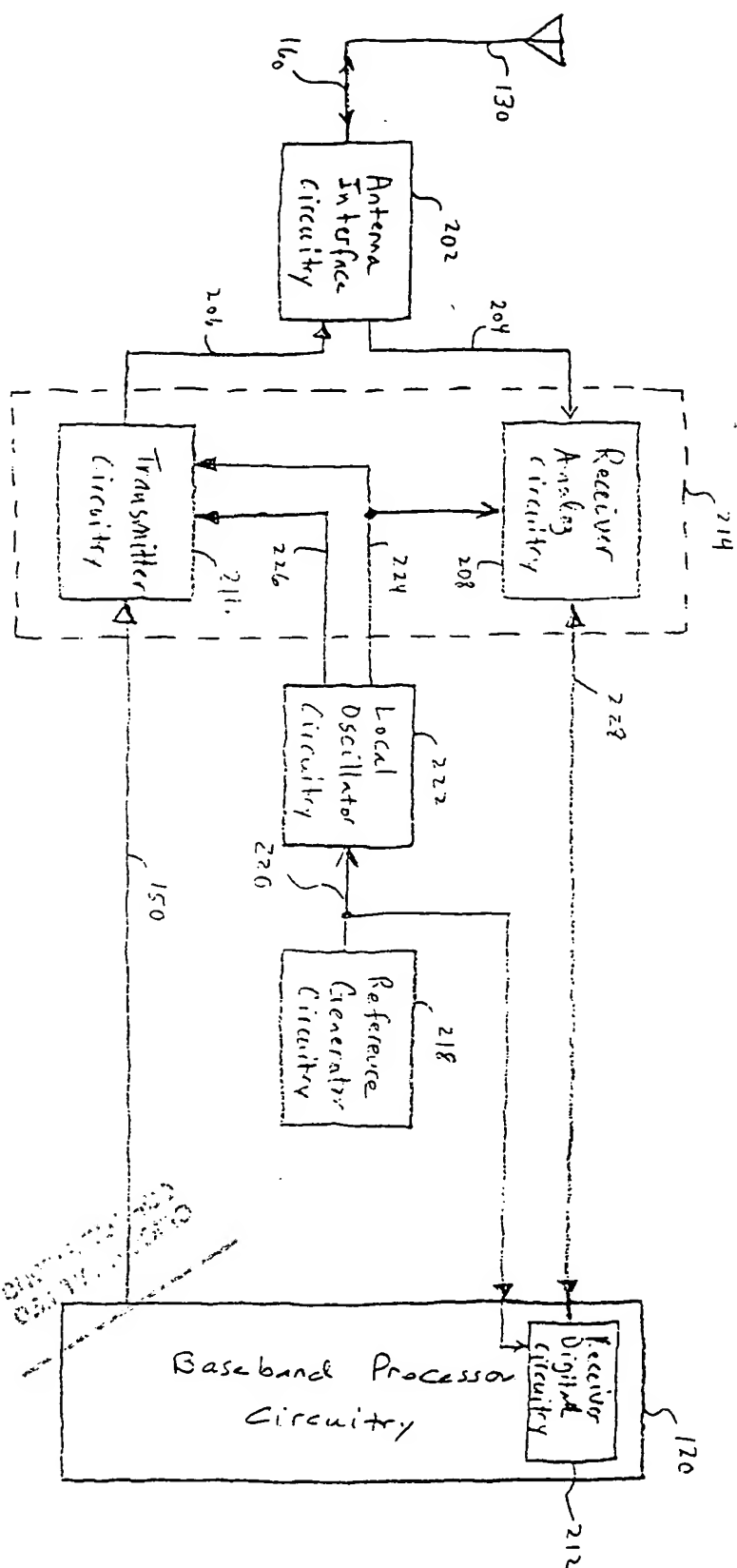


FIG. 2C

FIG. 2D

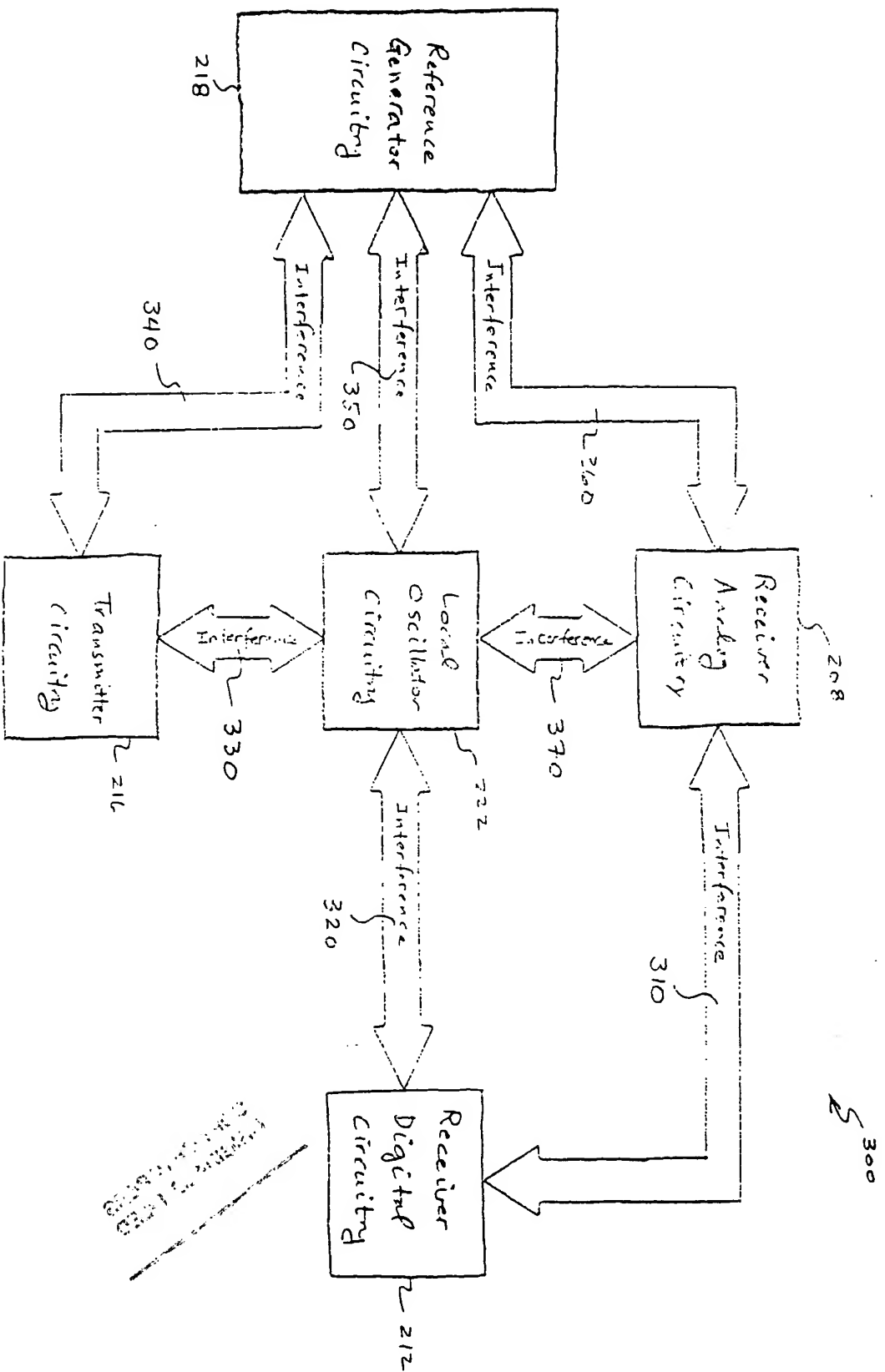


FIG. 3

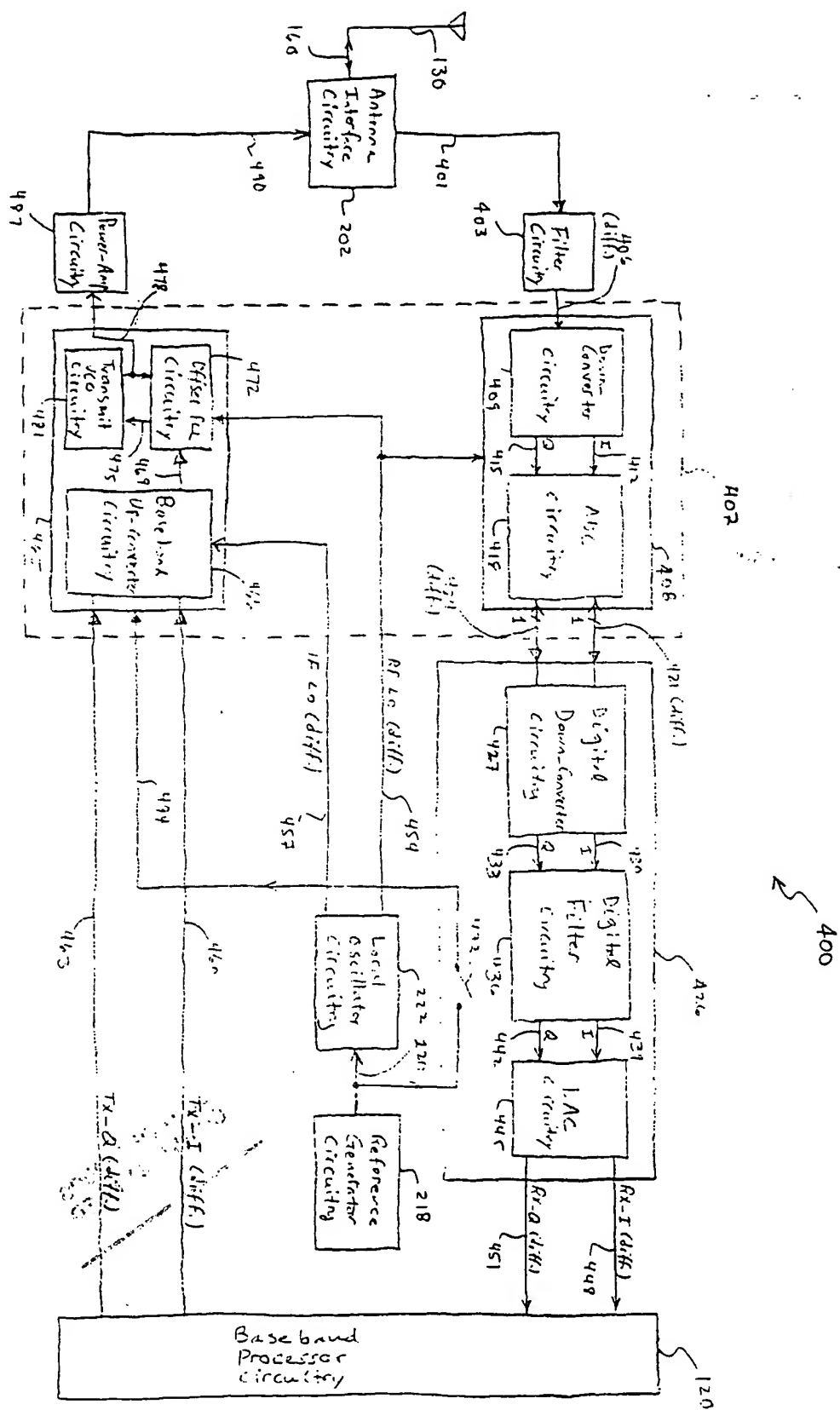


FIG. 4

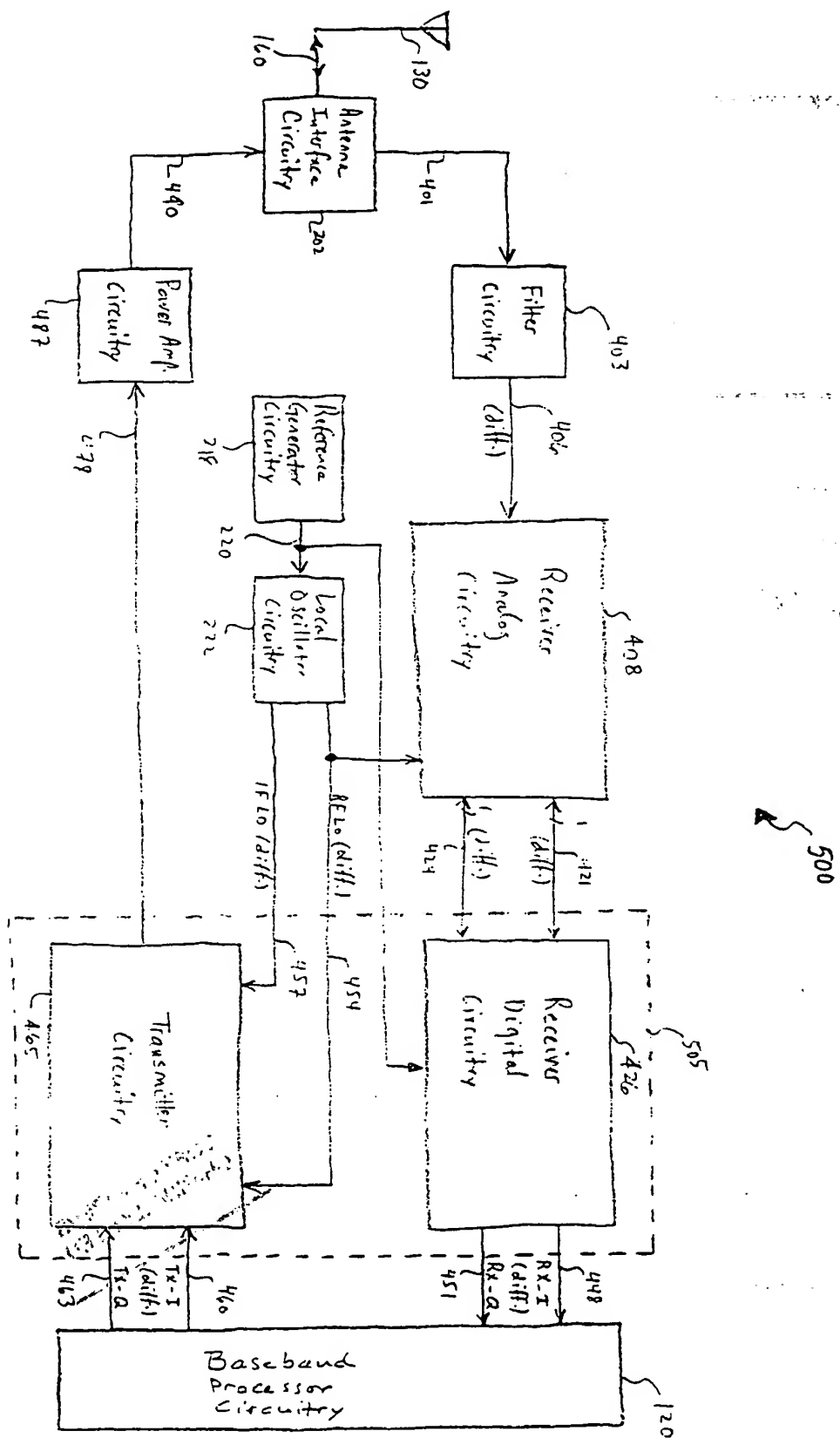


FIG. 5

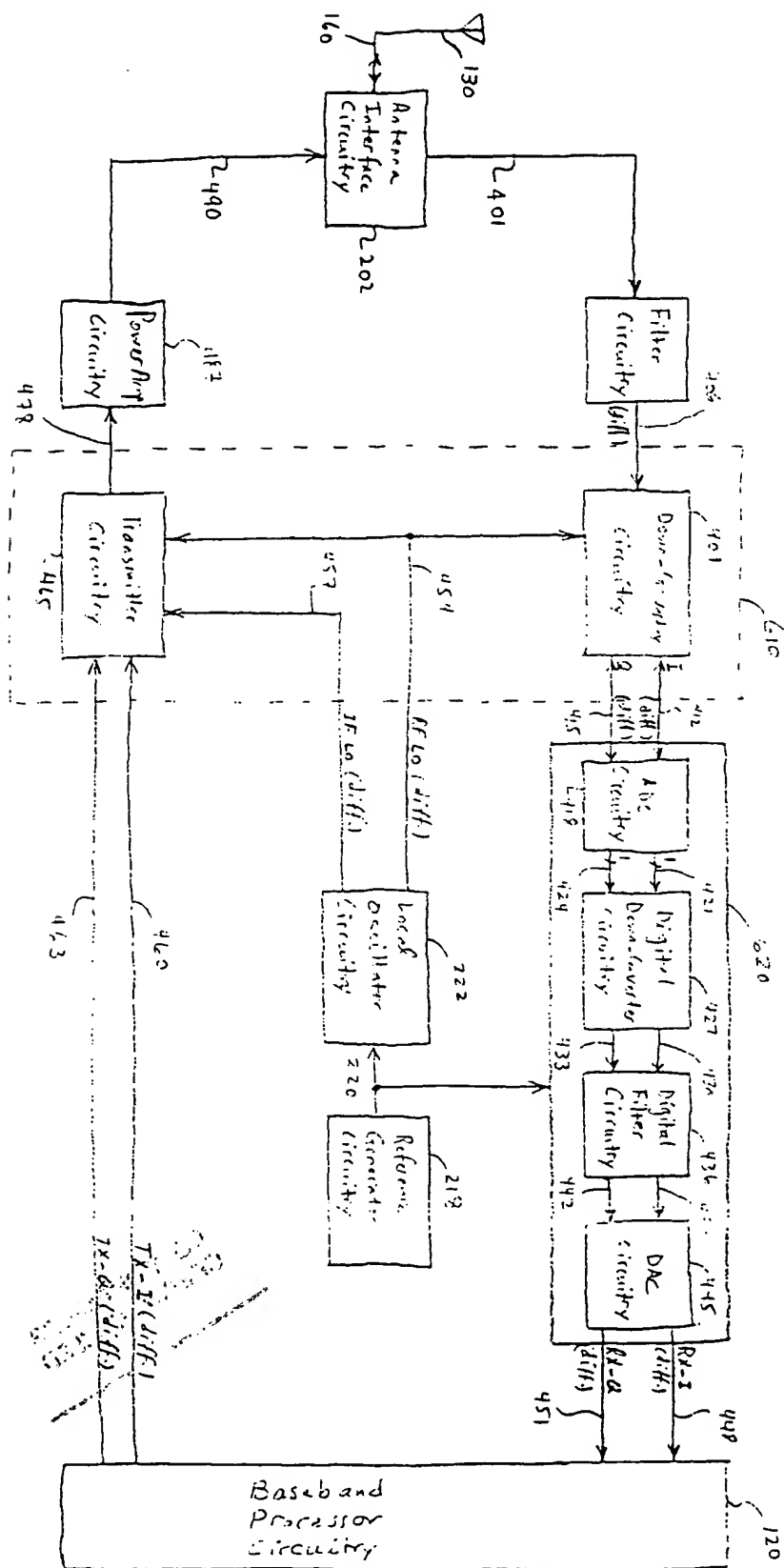


FIG. 6

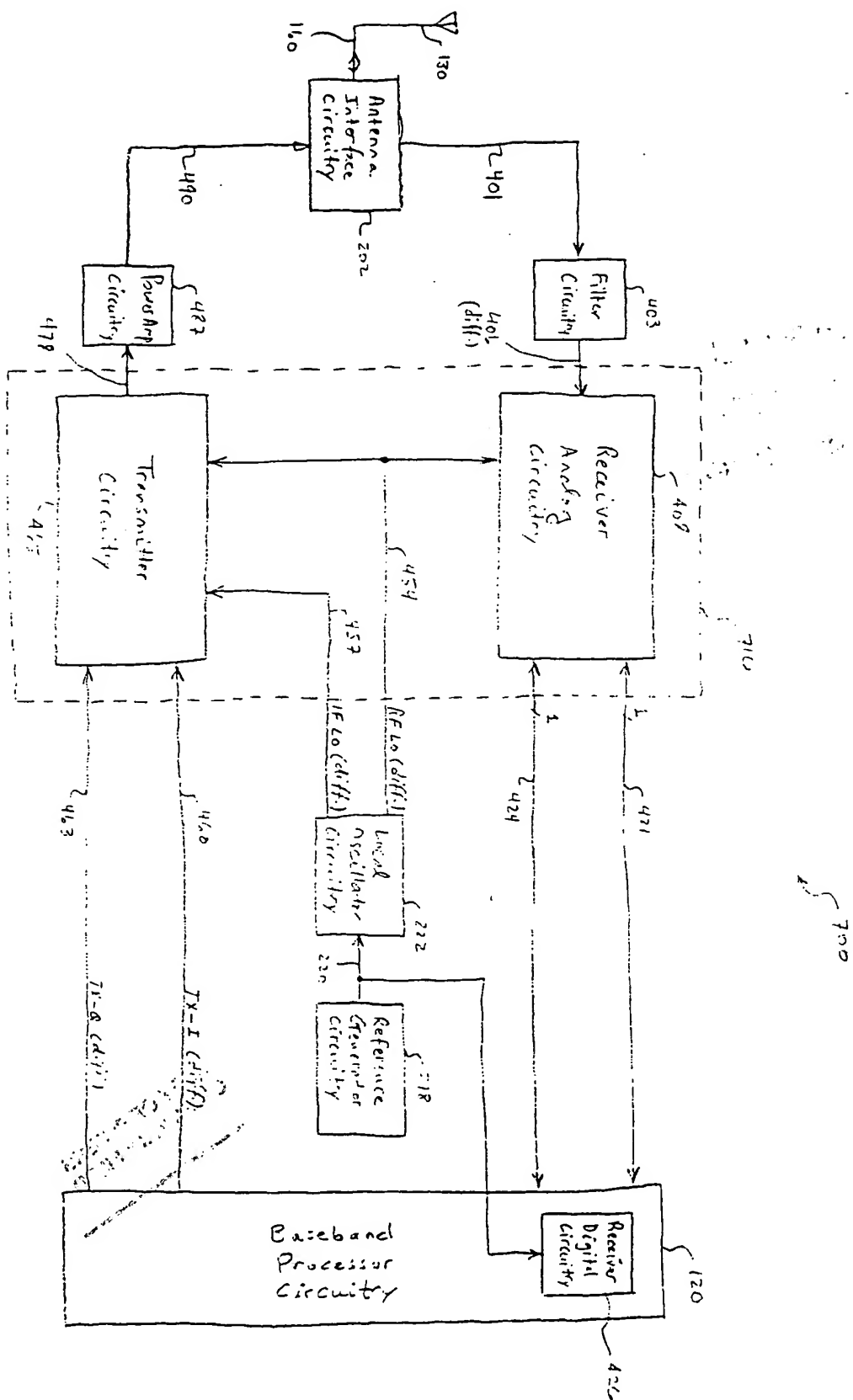
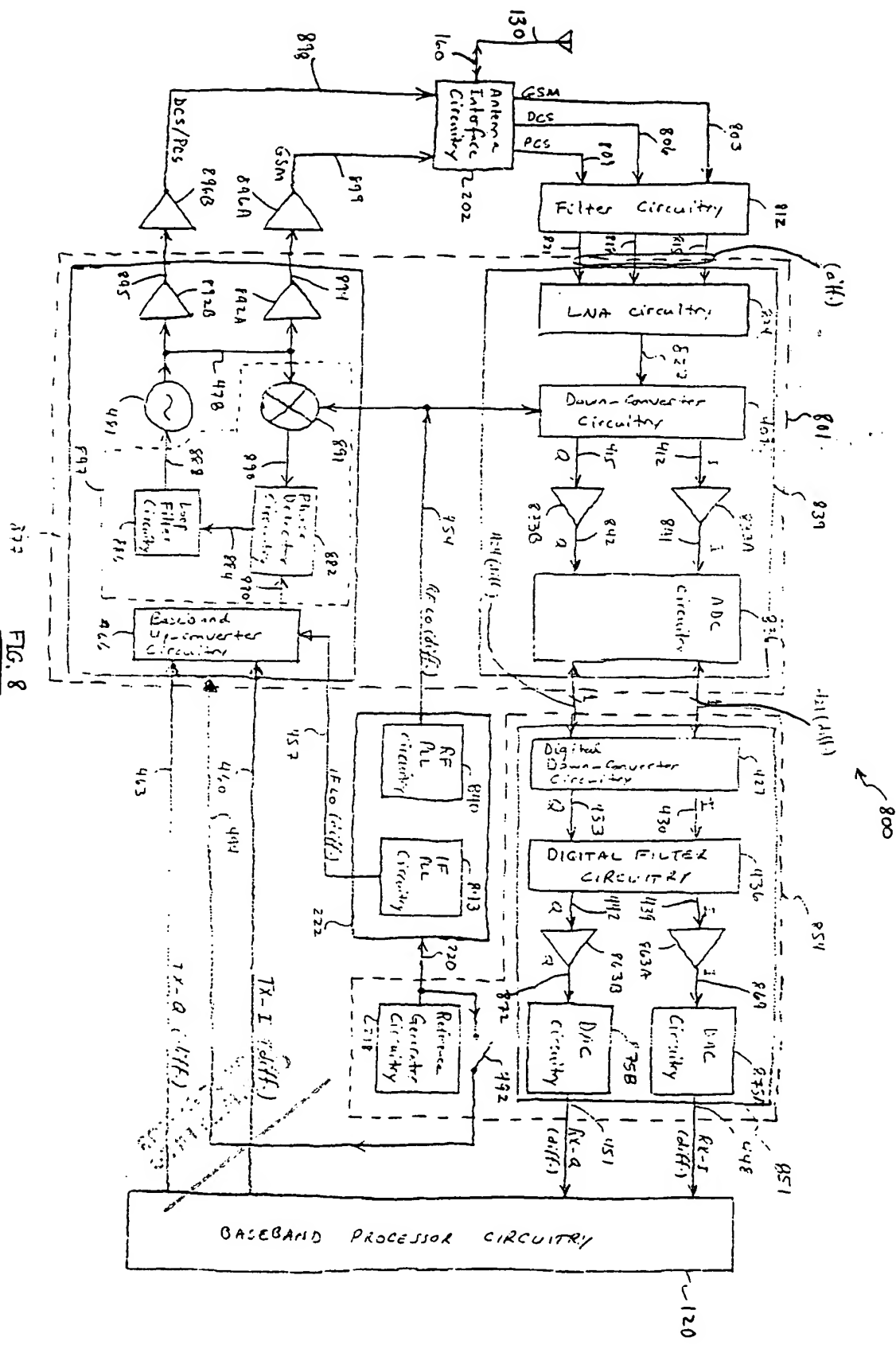


FIG. 7



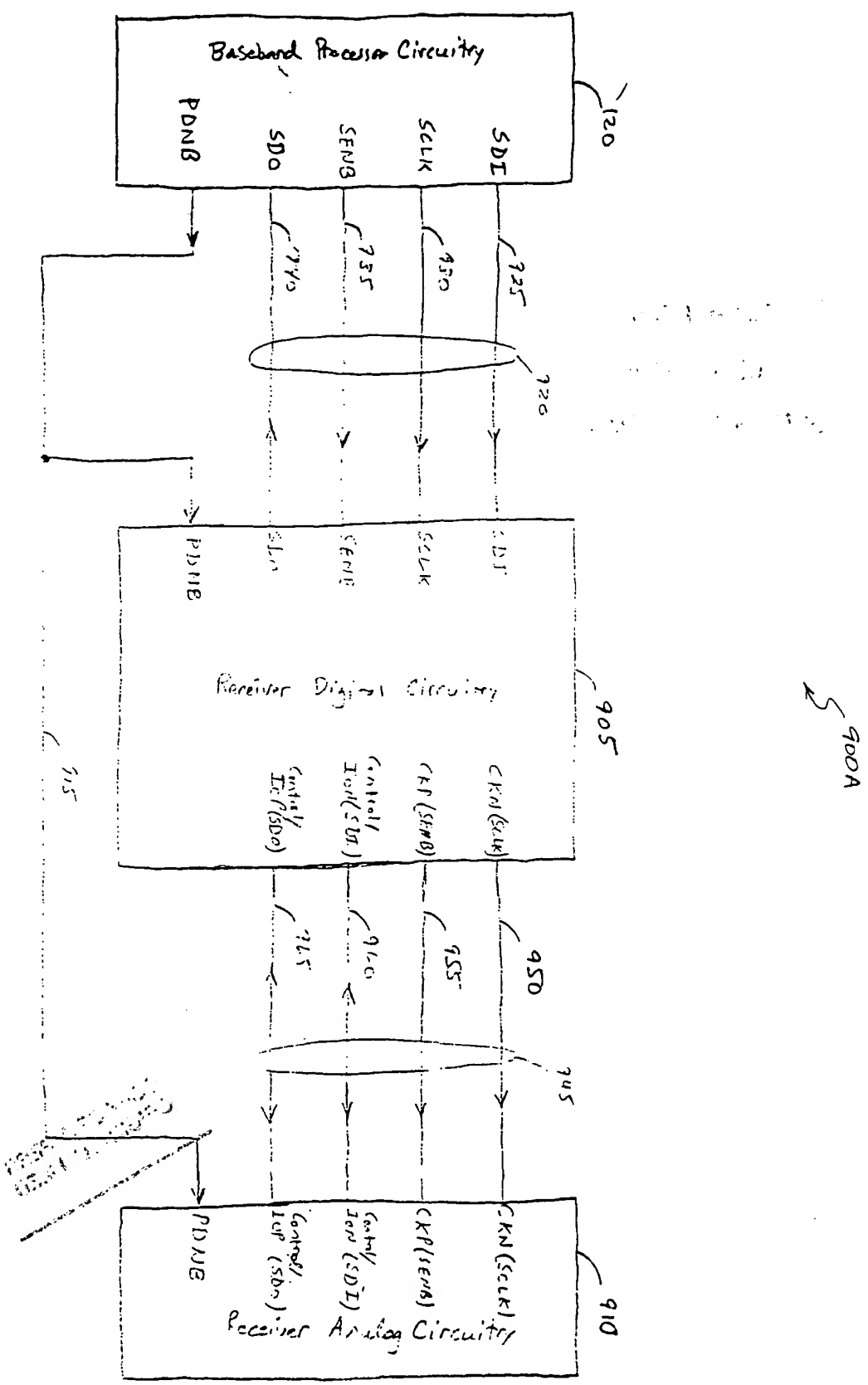


FIG. 9A

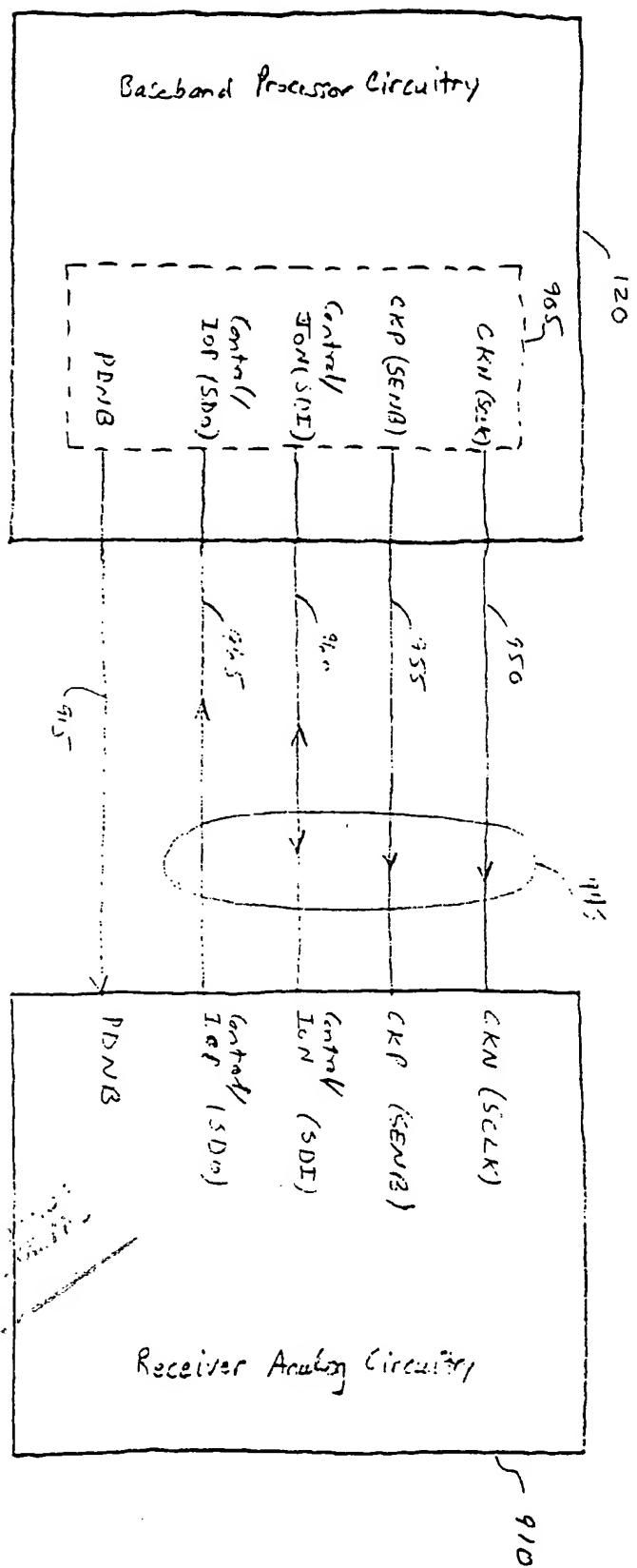


FIG. 9B

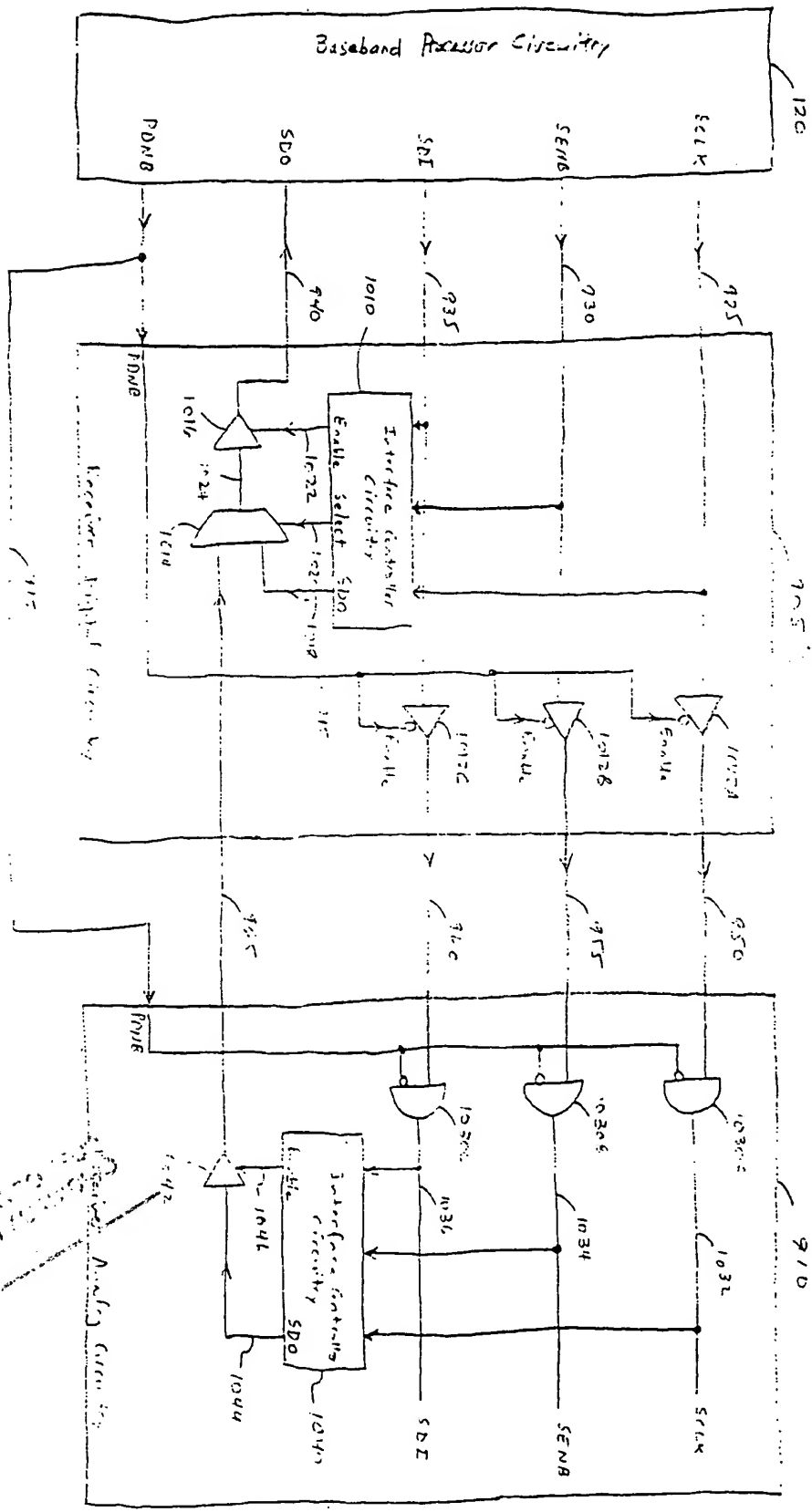


FIG. 10

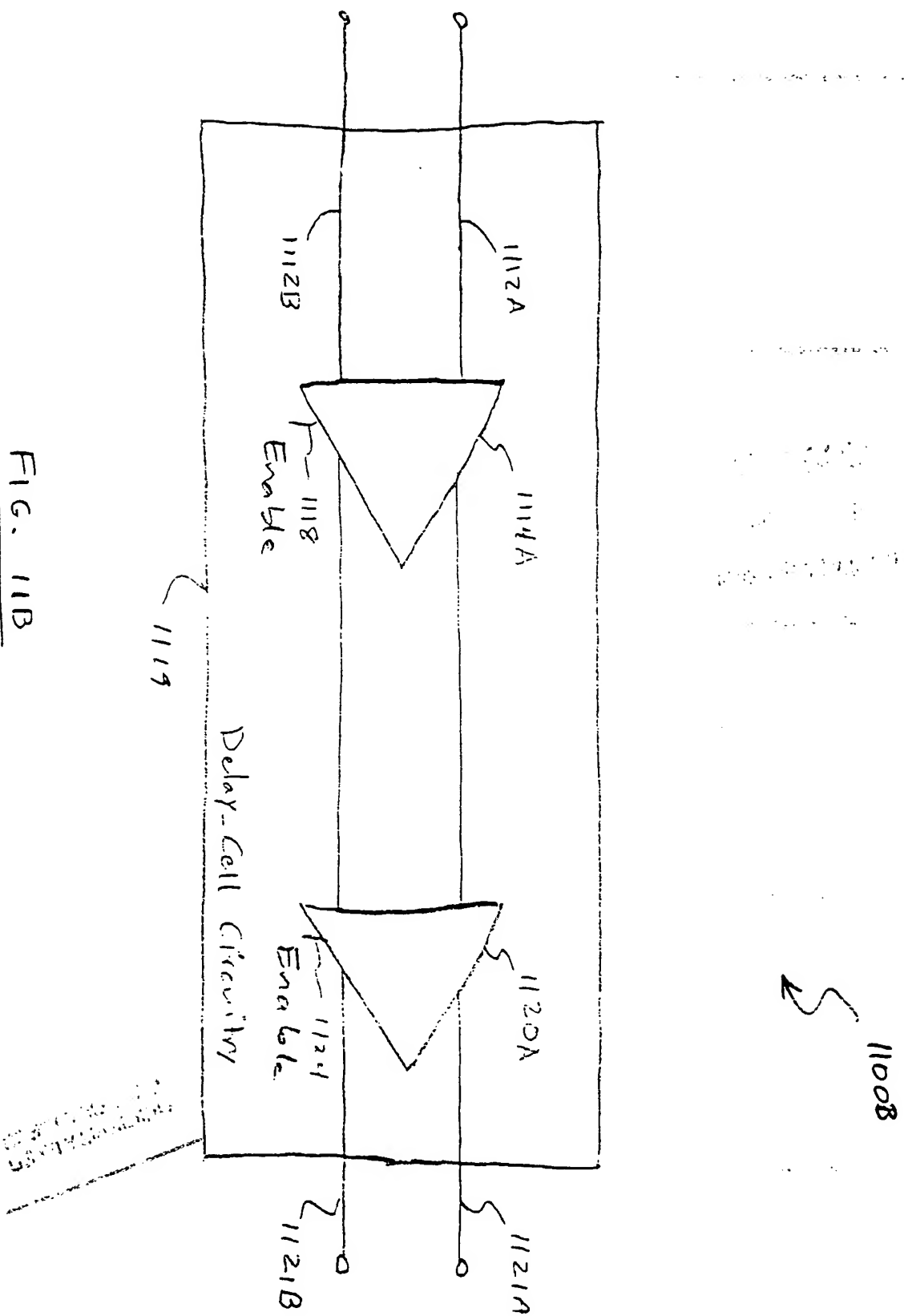


FIG. 11B

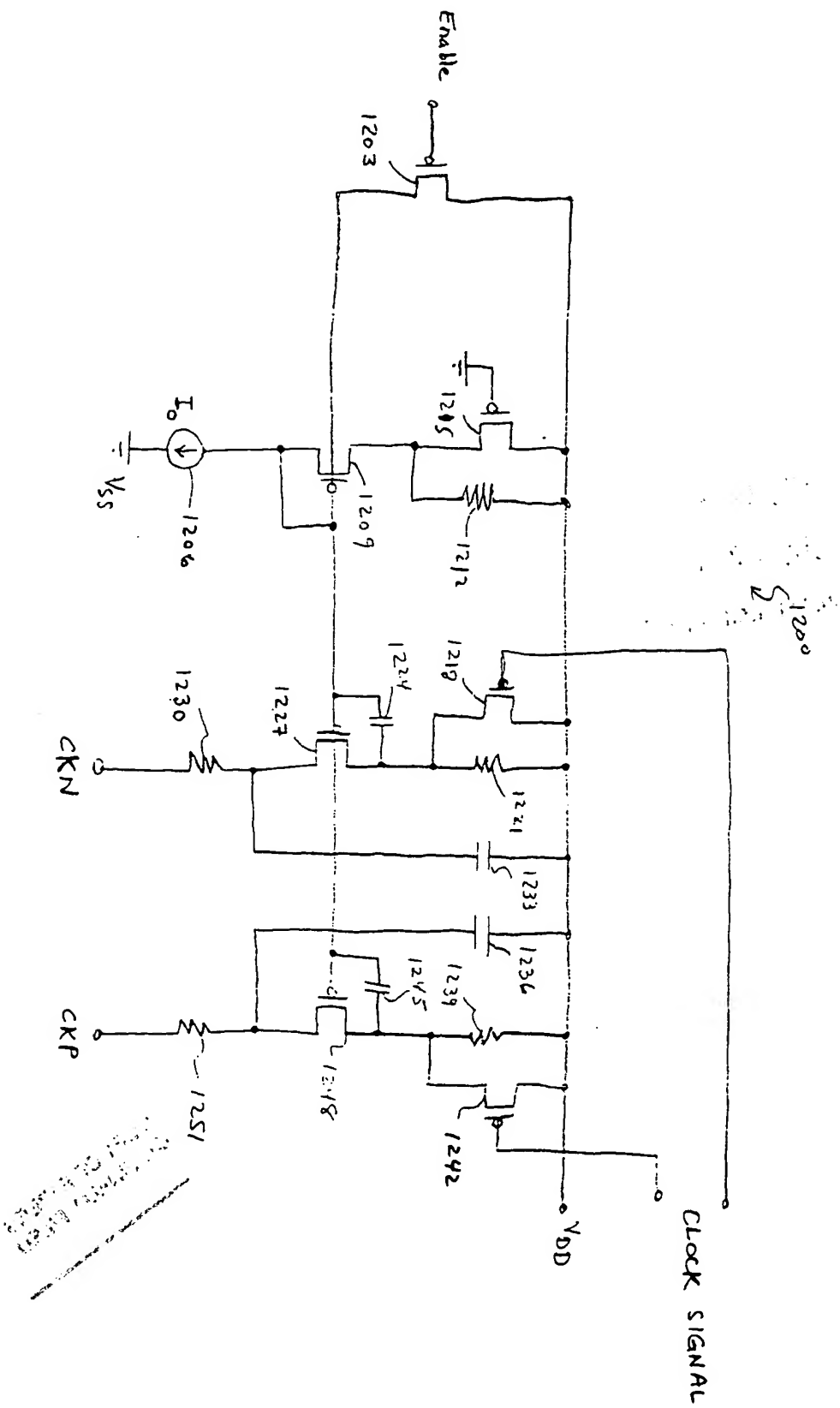


FIG. 12

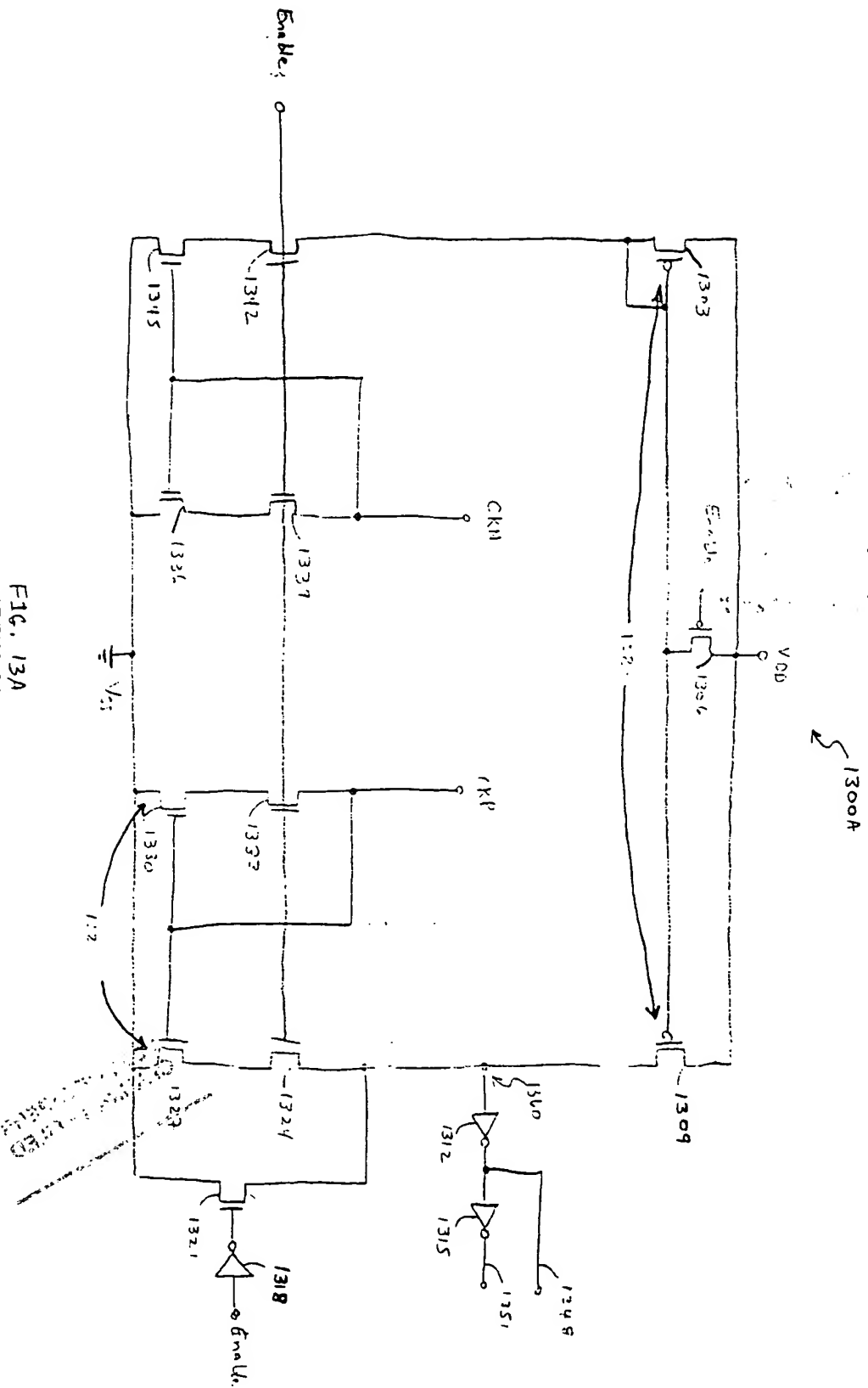


FIG. 13A

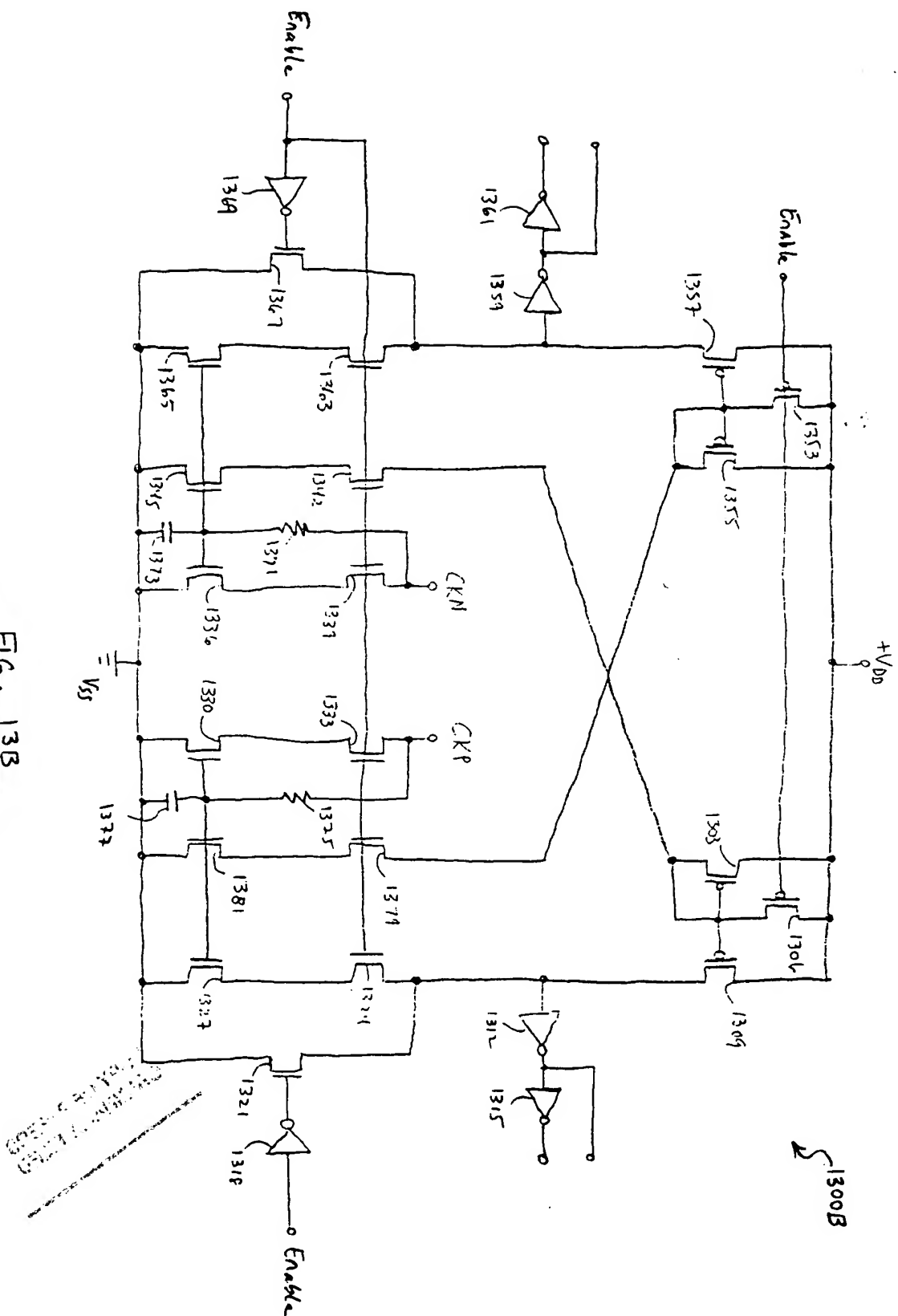


FIG. 13B

1400

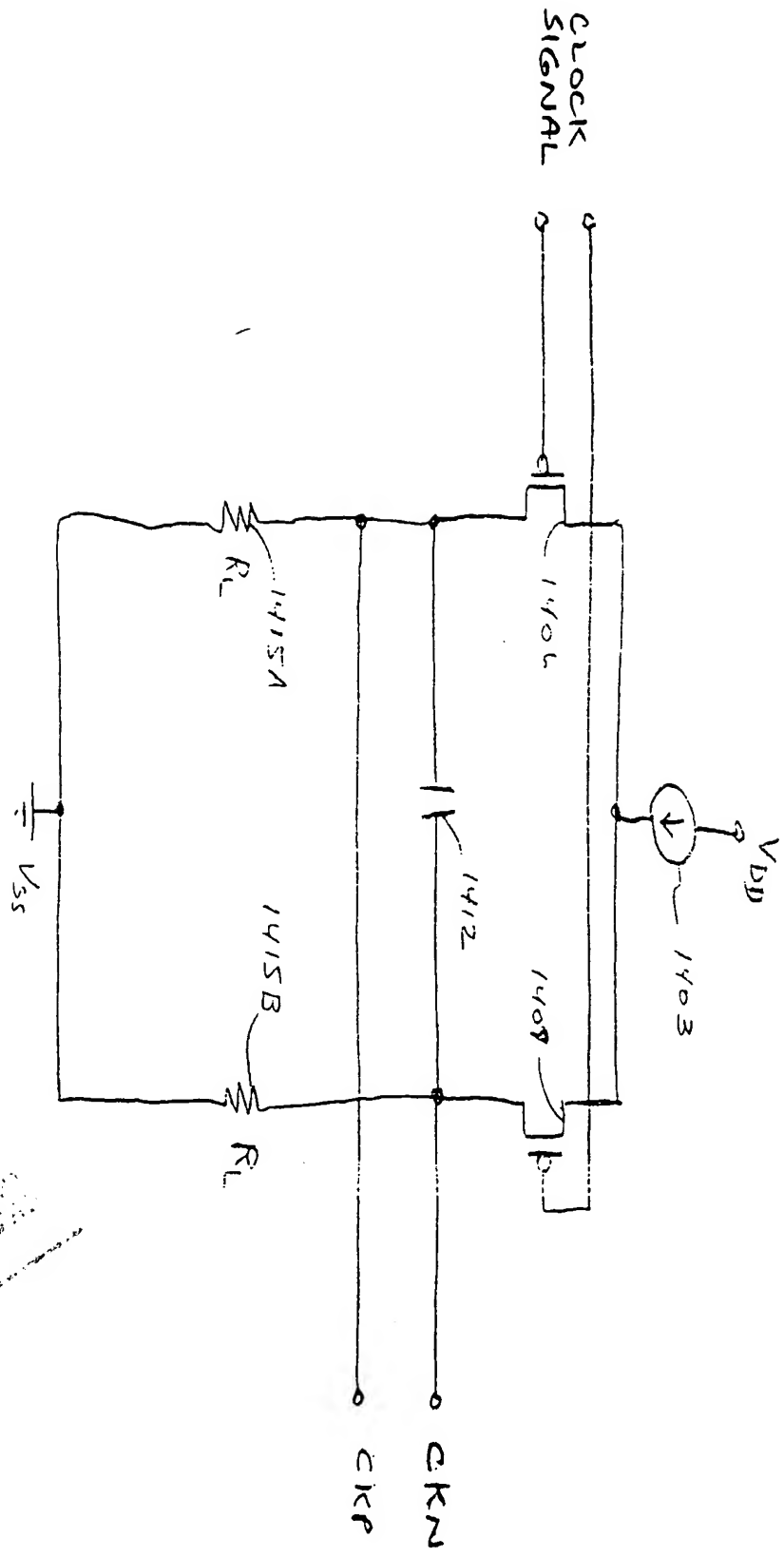


FIG. 14

1400

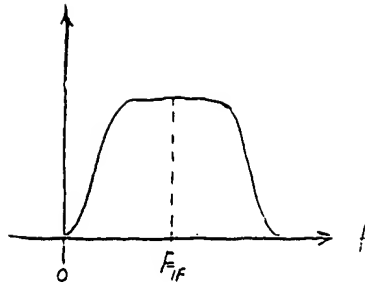


FIG. 15

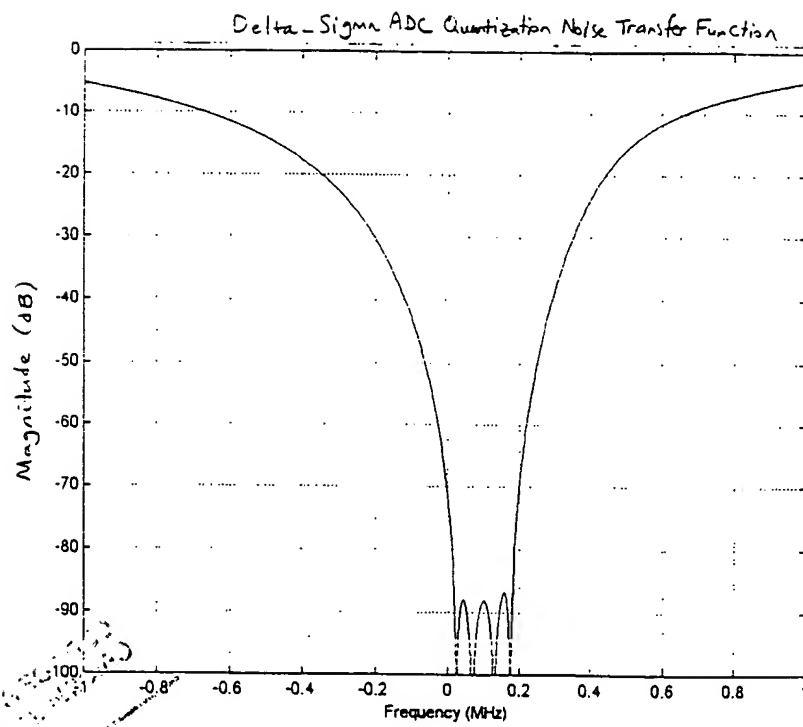


FIG. 16

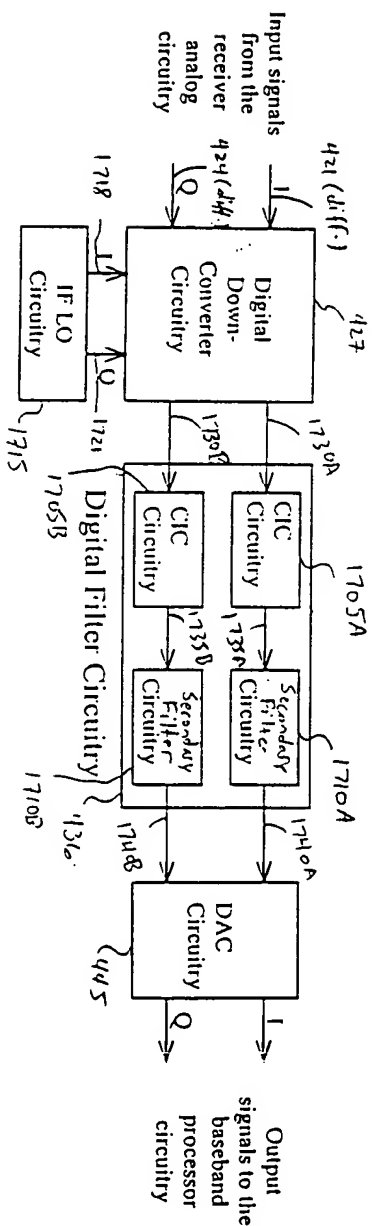


FIG. 17A

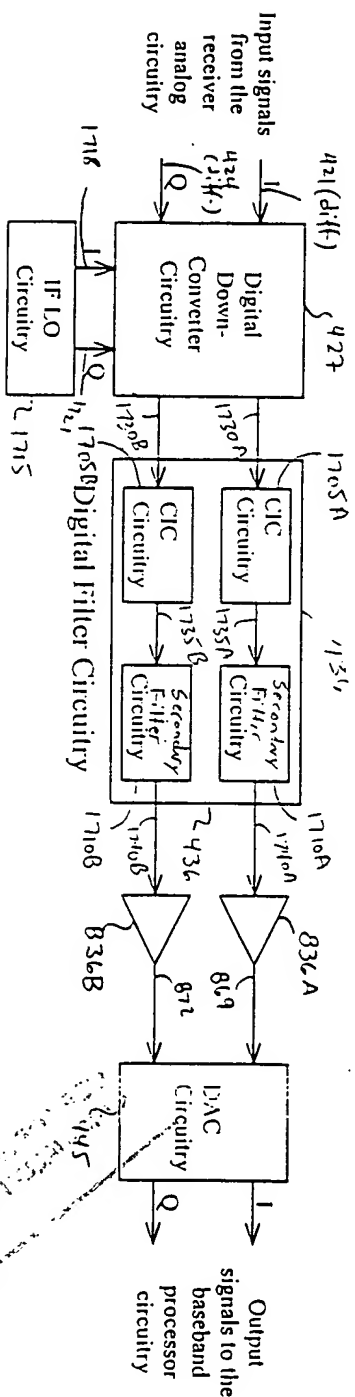


FIG. 17B

FIG. 17A and FIG. 17B are schematic diagrams of a signal processing system.

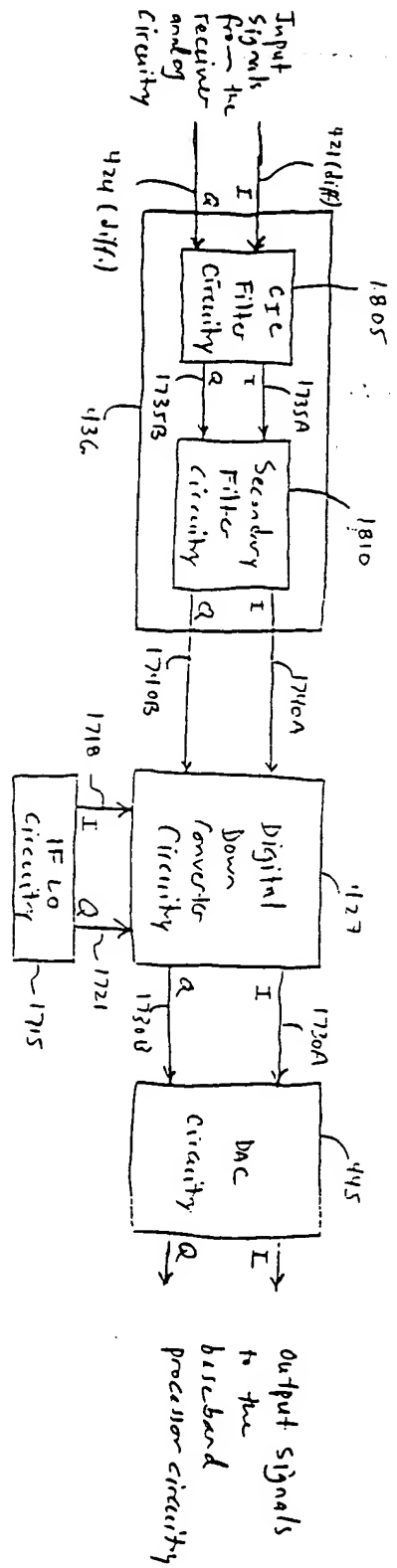


FIG. 18A

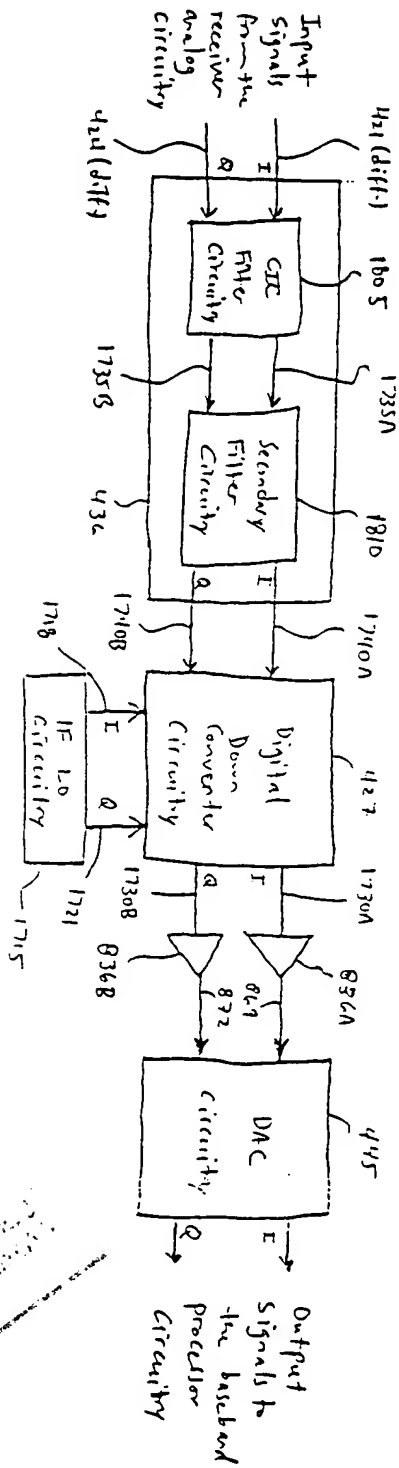


FIG. 18B

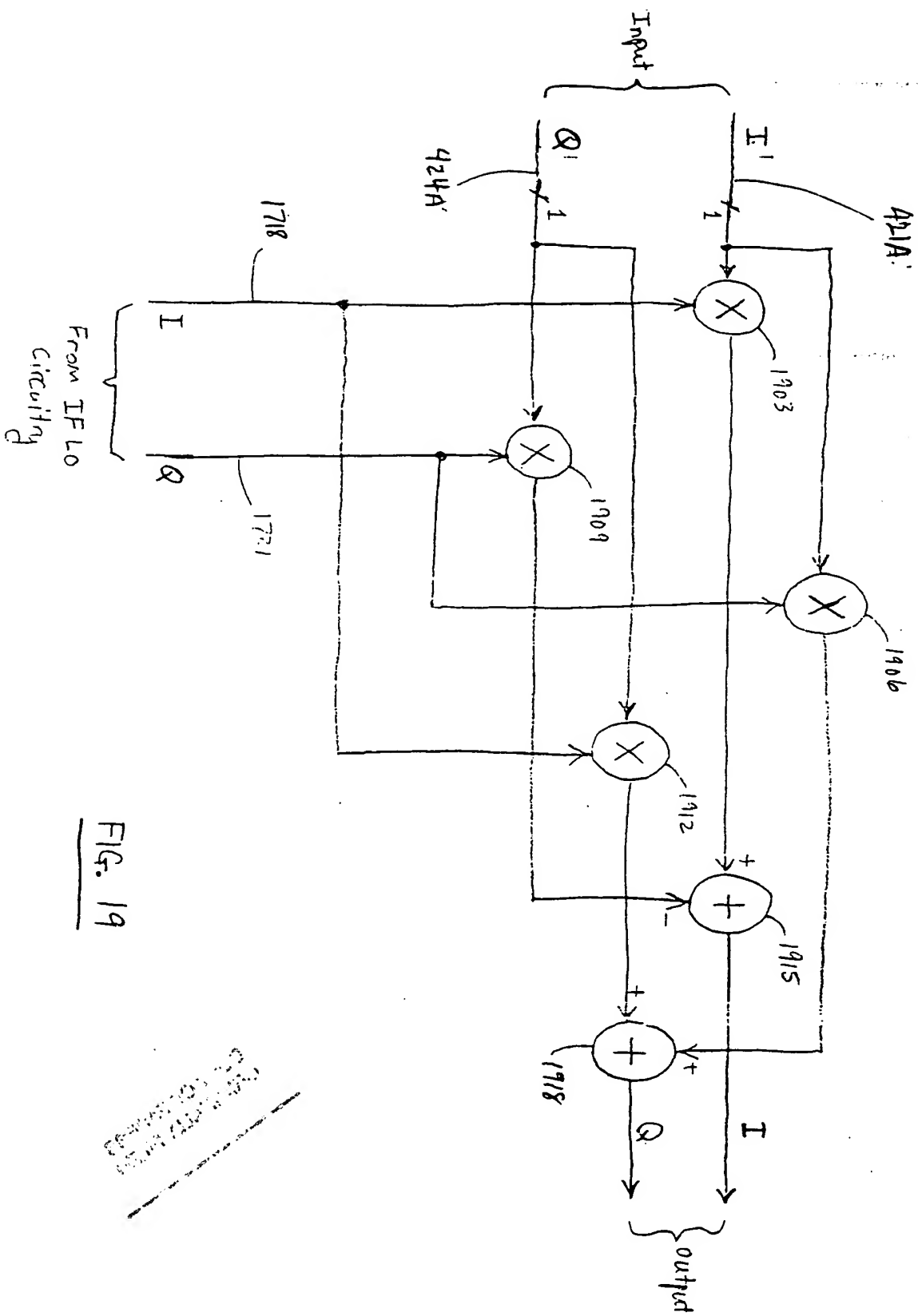


FIG. 19

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10/10/77

1715

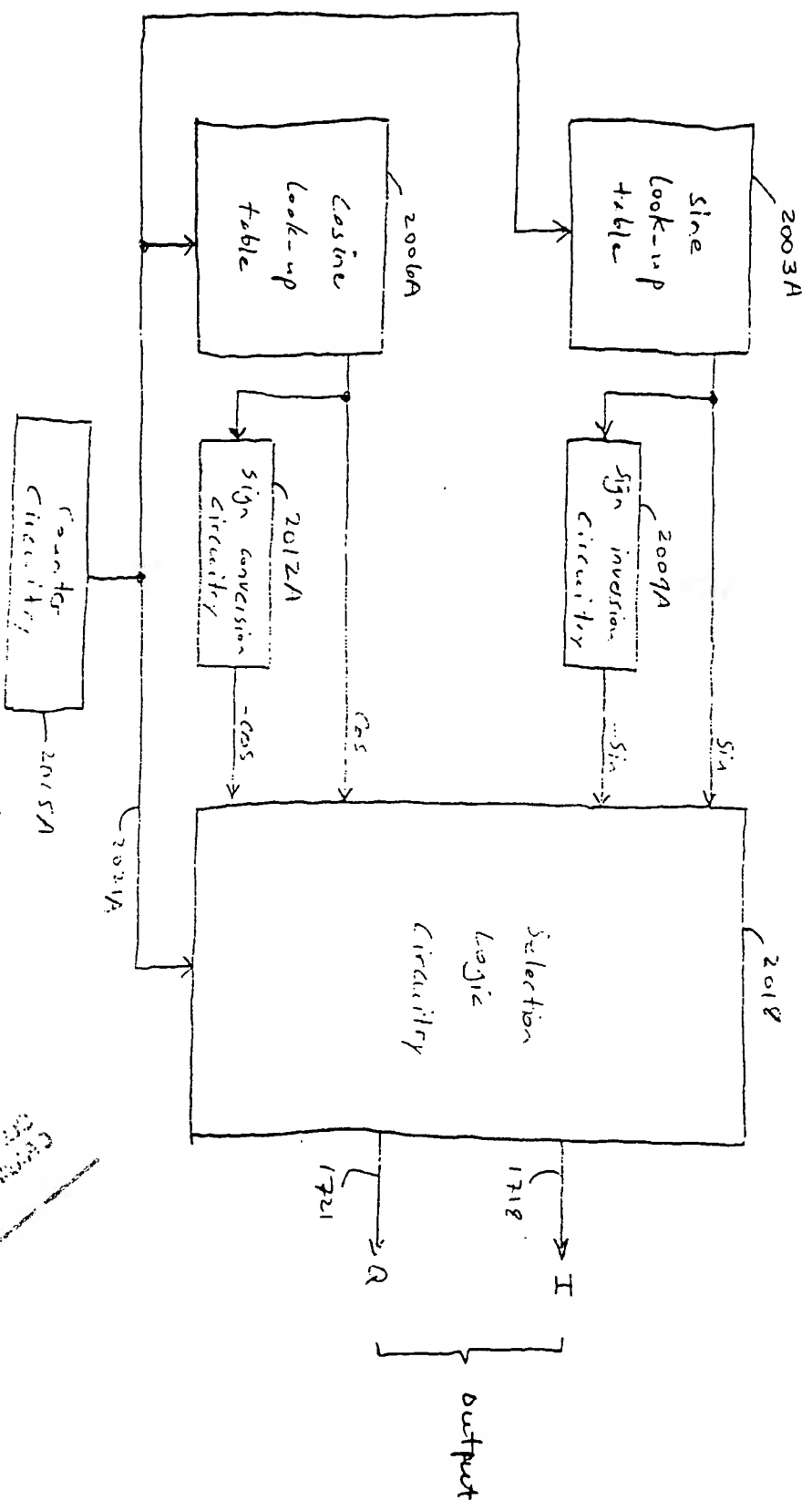


FIG. 20A

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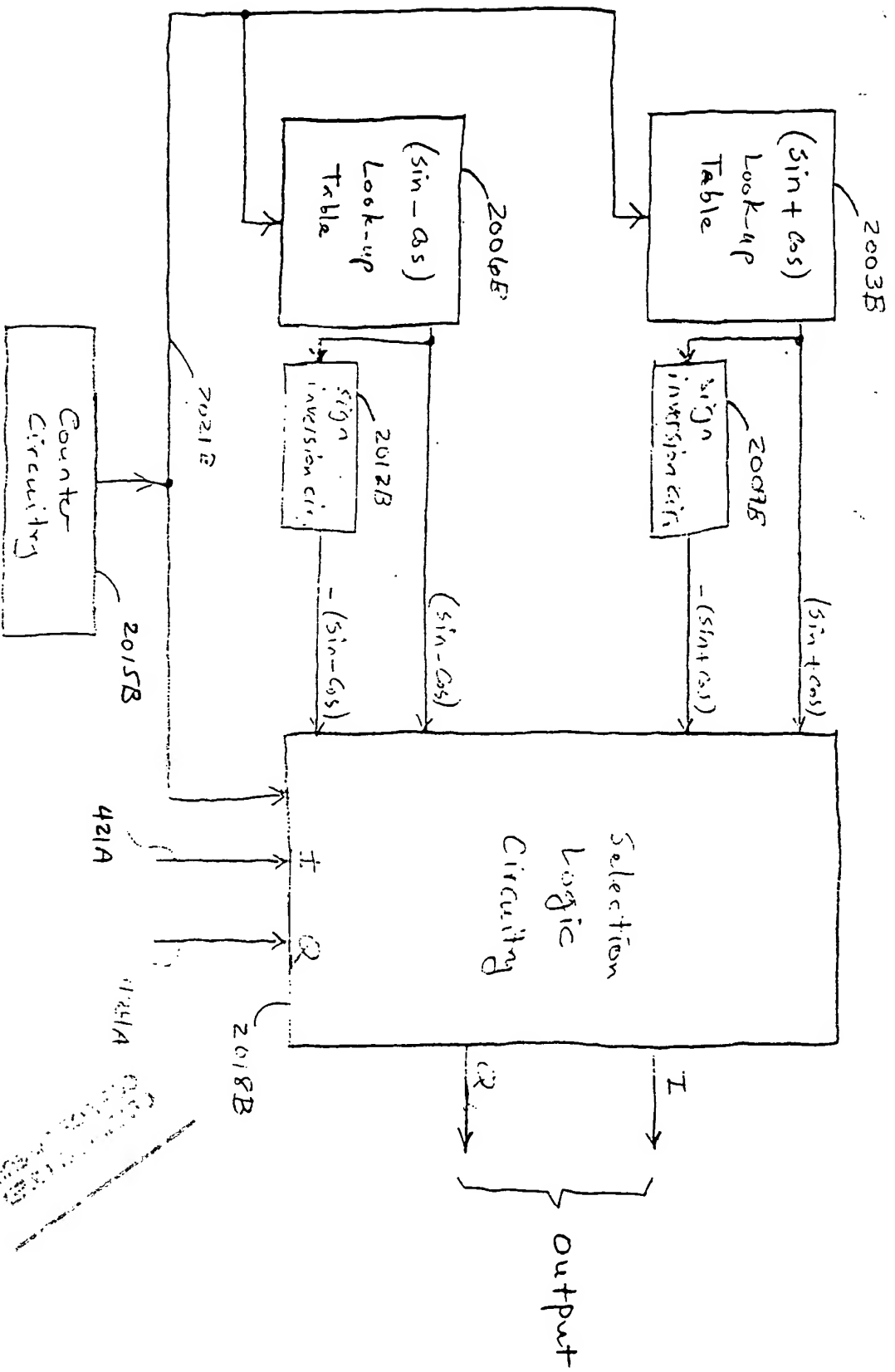


FIG. 20B

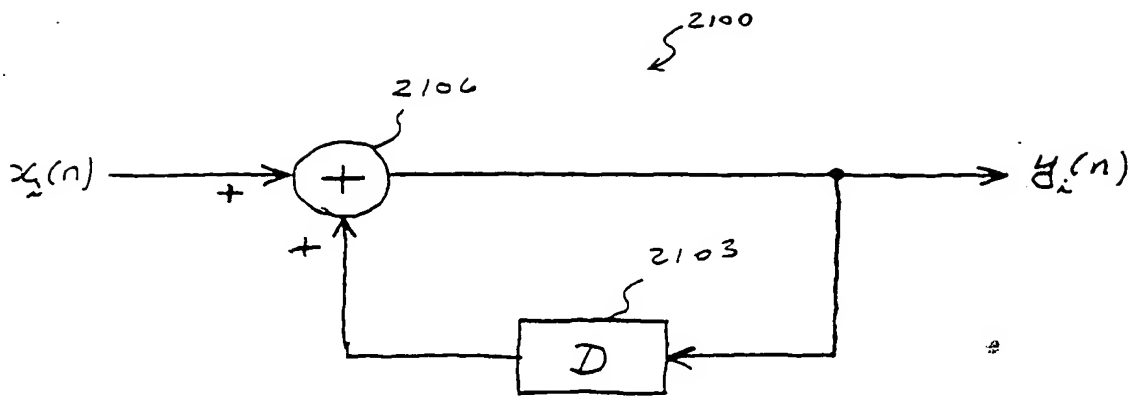


FIG. 21

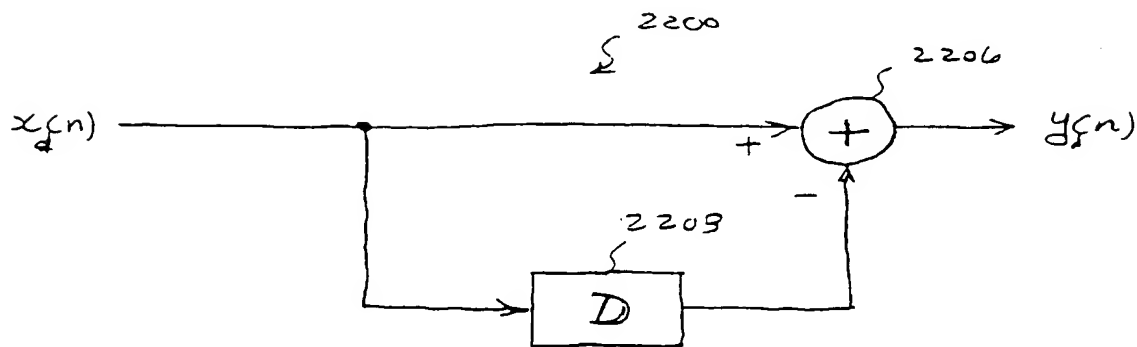


FIG. 22

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 DATE 11-15-2013

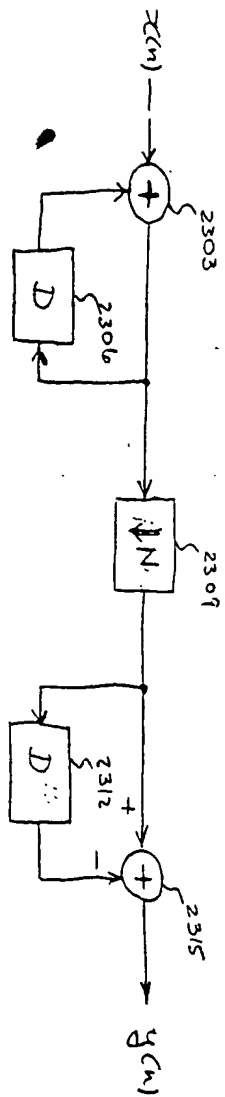


FIG. 23

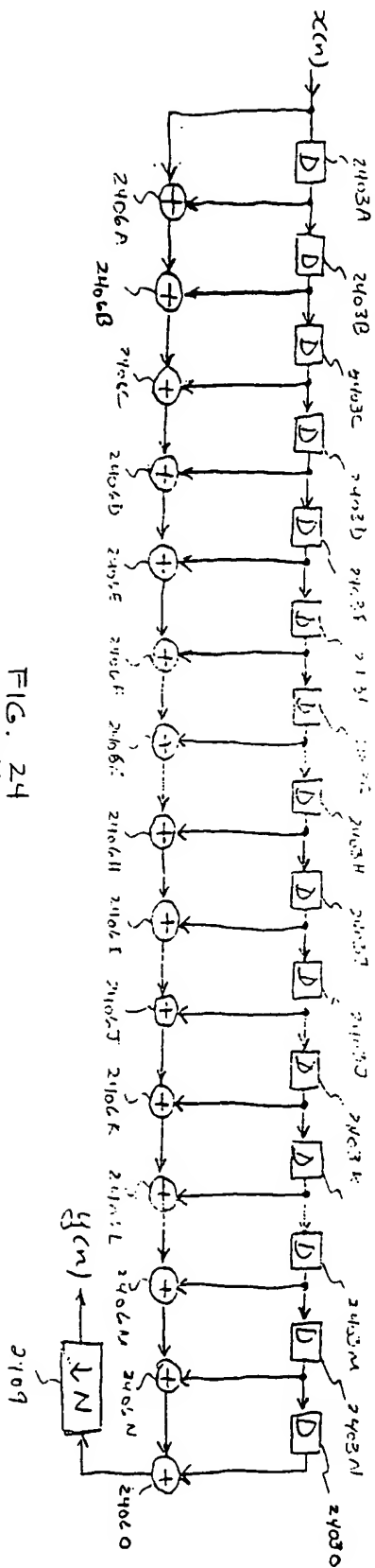


FIG. 24

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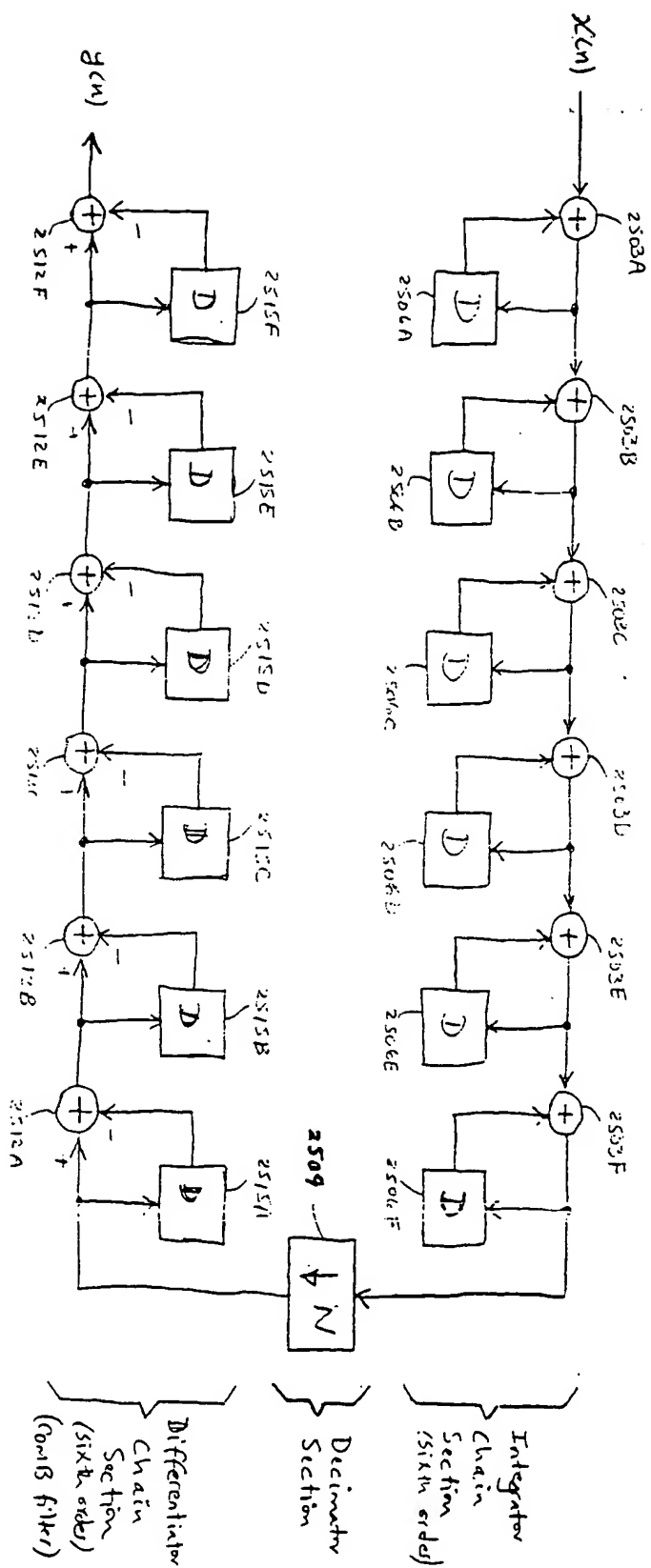


FIG. 25

U.S. Pat. 4,111,111
 Dec. 2, 1978
 Filed May 1, 1977

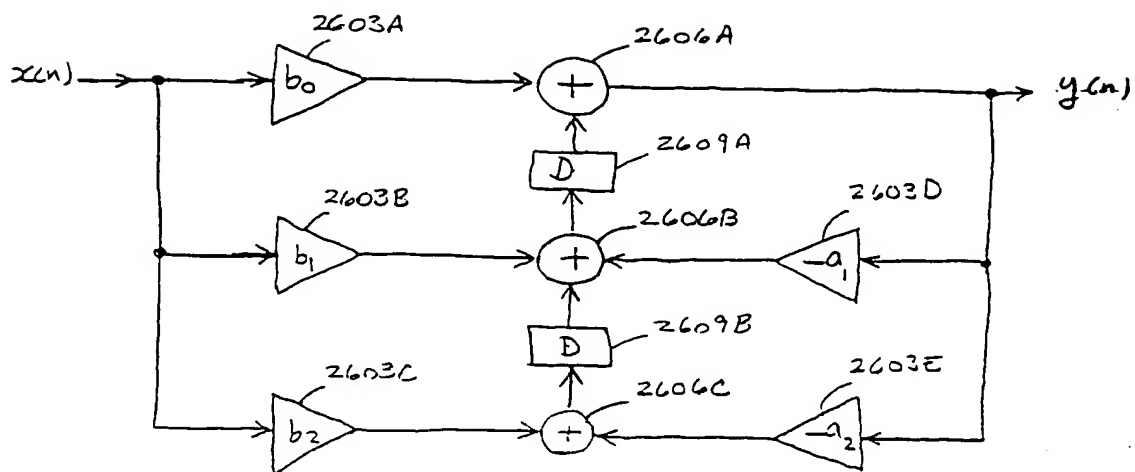


FIG. 26

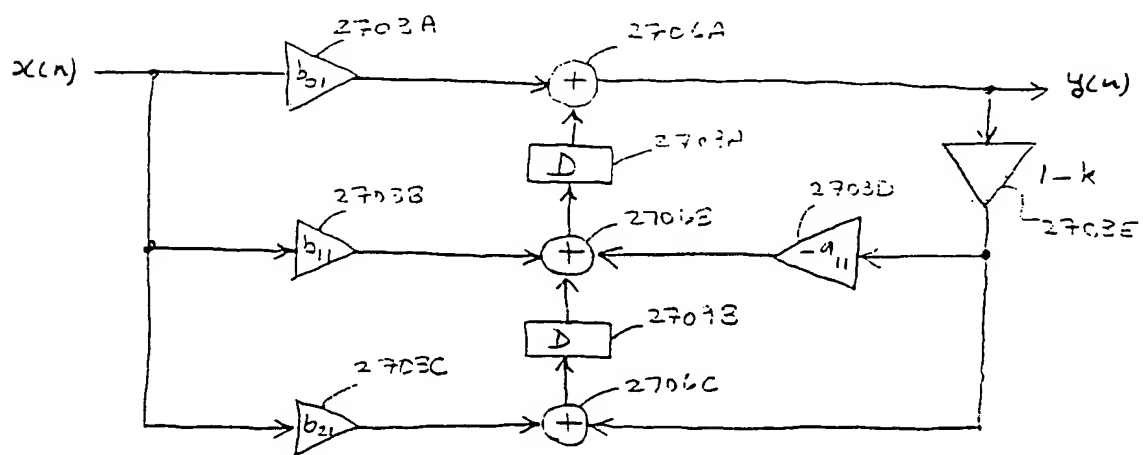
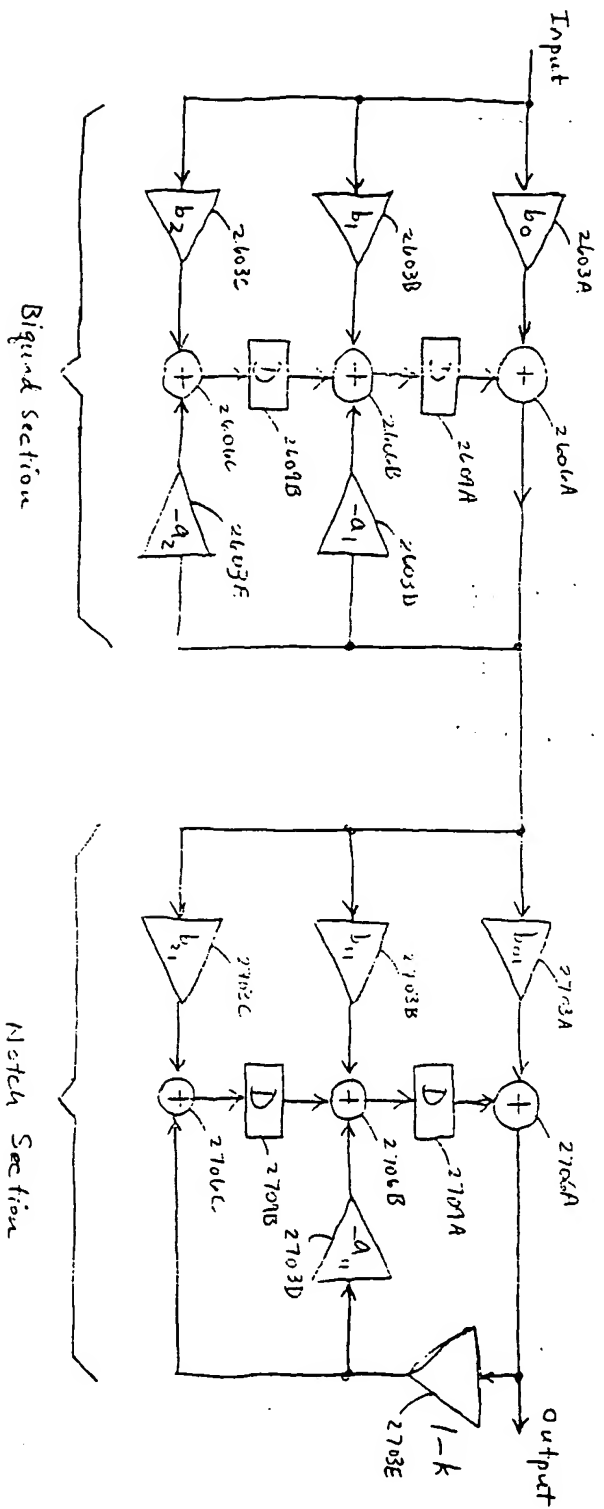


FIG. 27

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2703A 2703B 2703C 2703D 2703E 2703F 2704A 2704B 2704C 2709A 2709B 2709C 2709D 2709E 2709F 2709G 2709H 2709I 2709J 2709K 2709L 2709M 2709N 2709O 2709P 2709Q 2709R 2709S 2709T 2709U 2709V 2709W 2709X 2709Y 2709Z

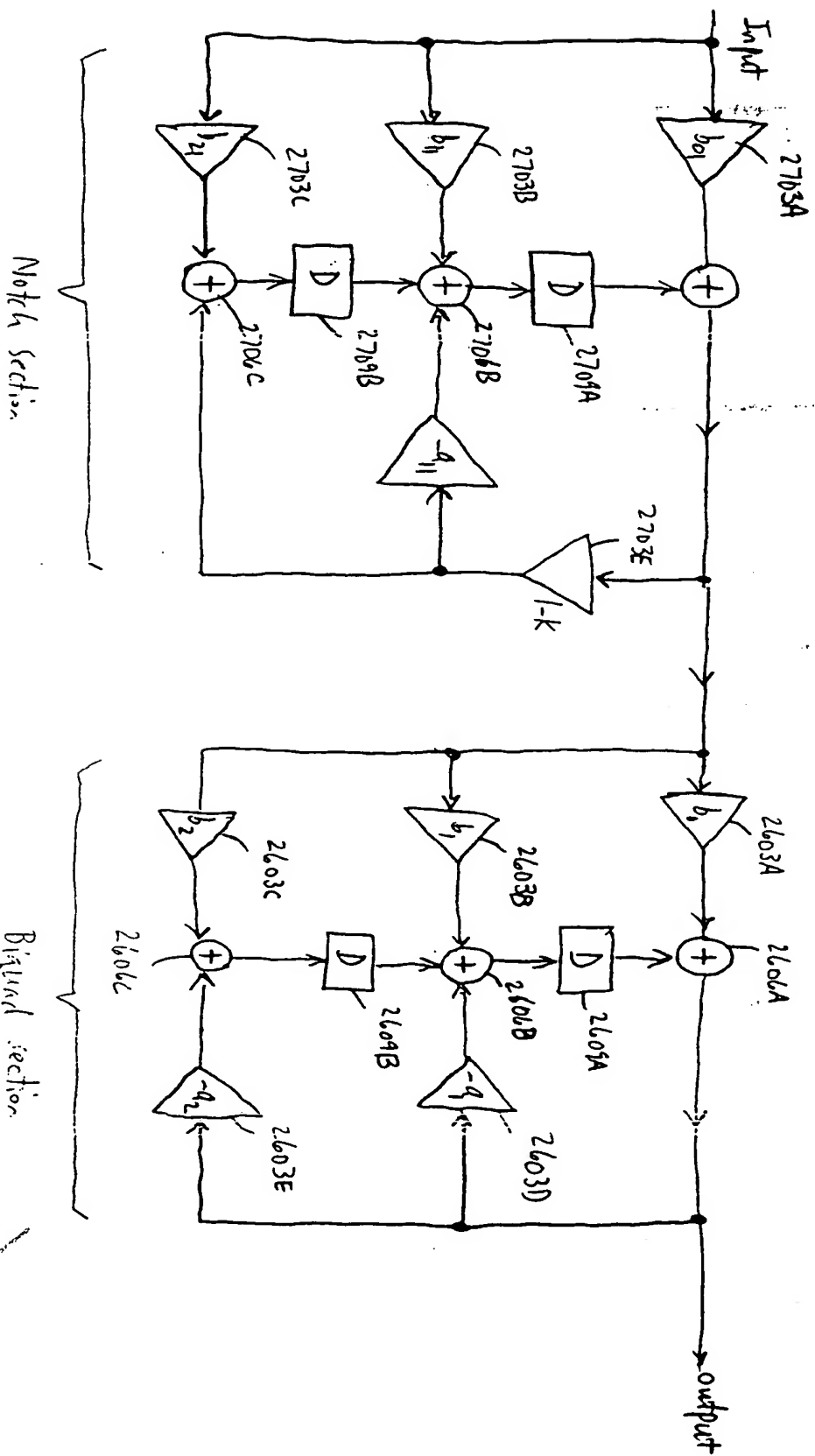


FIG. 28B

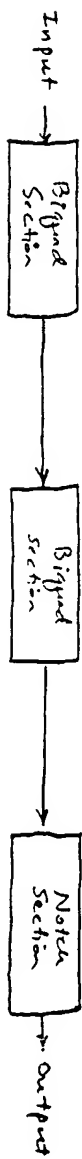


FIG. 29A



FIG. 29B



FIG. 29C

1. A method of processing an input signal to produce an output signal, comprising:
 a. providing a first BiQuad section;
 b. providing a second BiQuad section;
 c. providing a third BiQuad section;
 d. providing a fourth BiQuad section;
 e. providing a fifth BiQuad section;
 f. providing a Notch section;
 g. connecting the first BiQuad section to the second BiQuad section;
 h. connecting the second BiQuad section to the third BiQuad section;
 i. connecting the third BiQuad section to the fourth BiQuad section;
 j. connecting the fourth BiQuad section to the fifth BiQuad section;
 k. connecting the fifth BiQuad section to the Notch section;
 l. connecting the input signal to the first BiQuad section;
 m. connecting the output of the Notch section to the output signal.

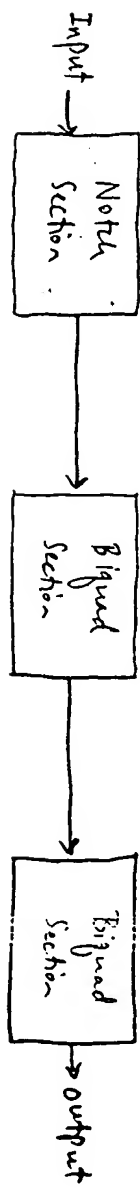


FIG. 29D



FIG. 29E

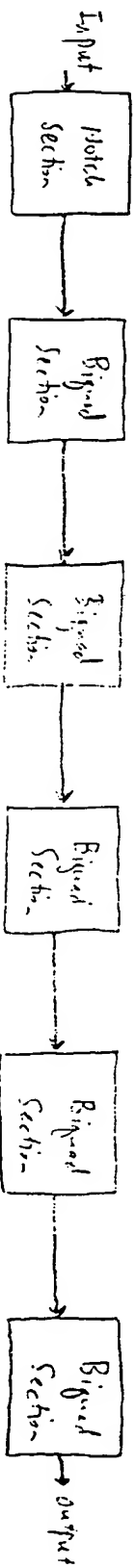


FIG. 29F

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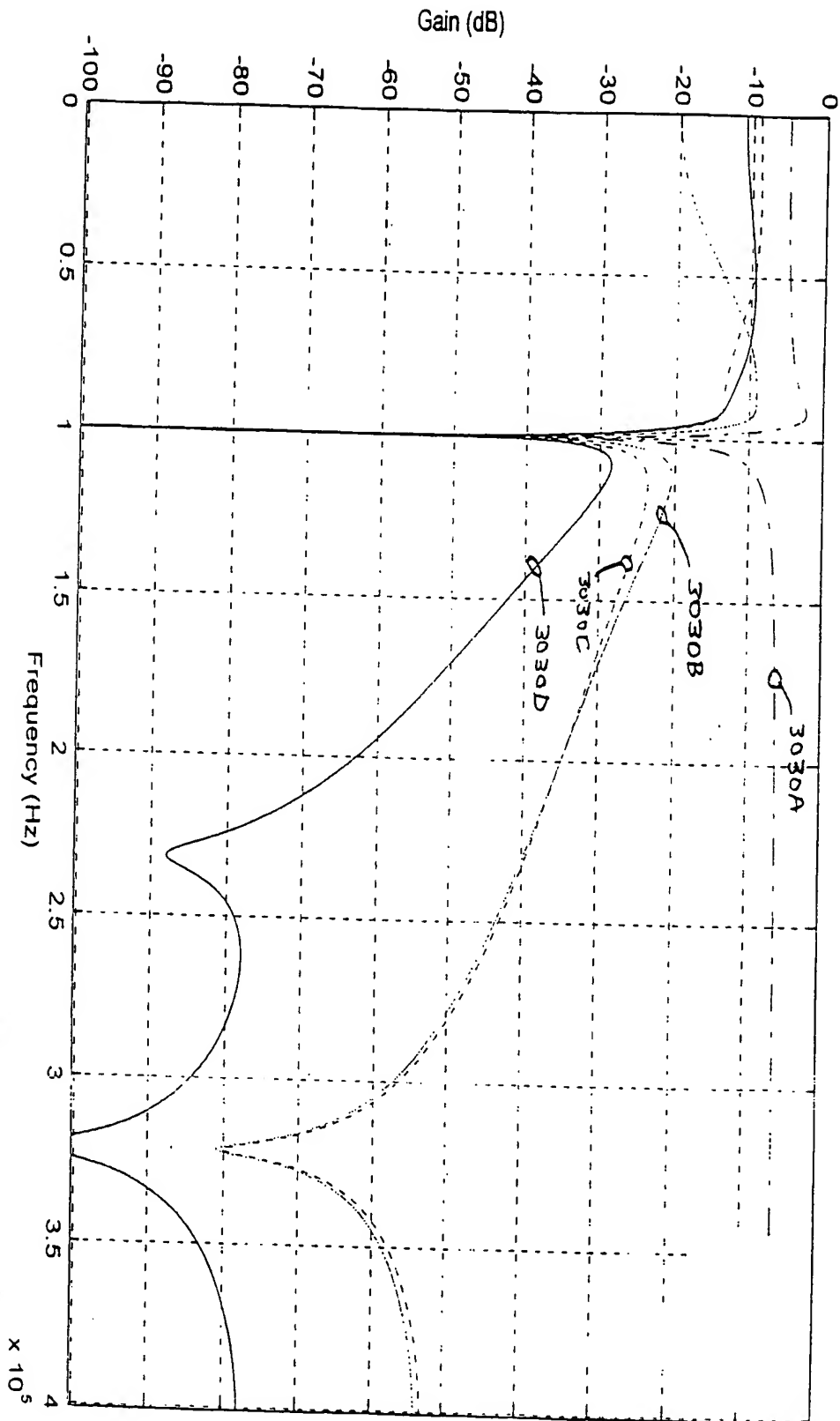


FIG. 30B

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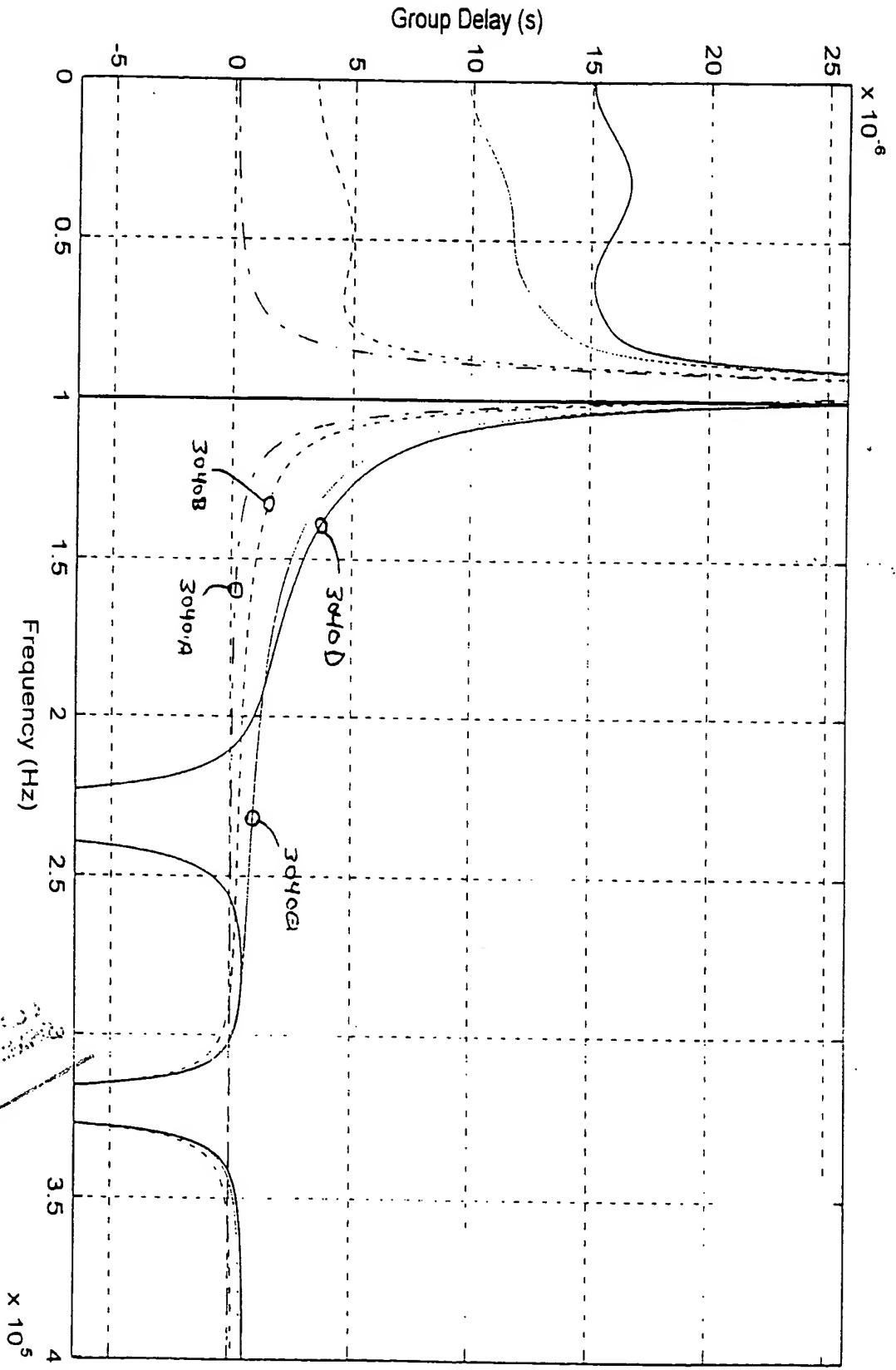


FIG. 30C

FIG. 31

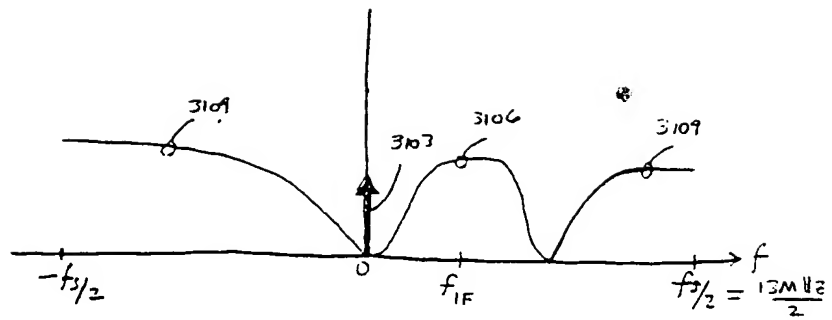


FIG. 32

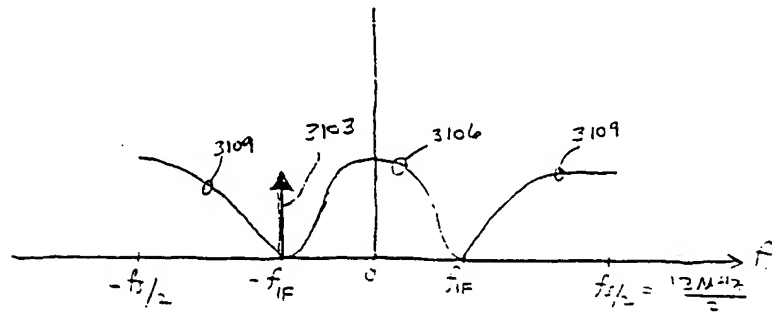


FIG. 33

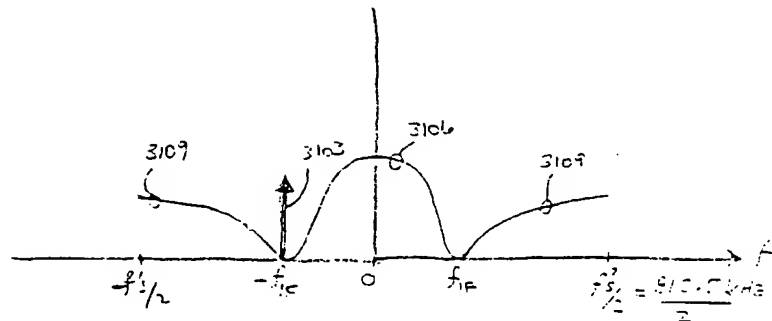


FIG. 34

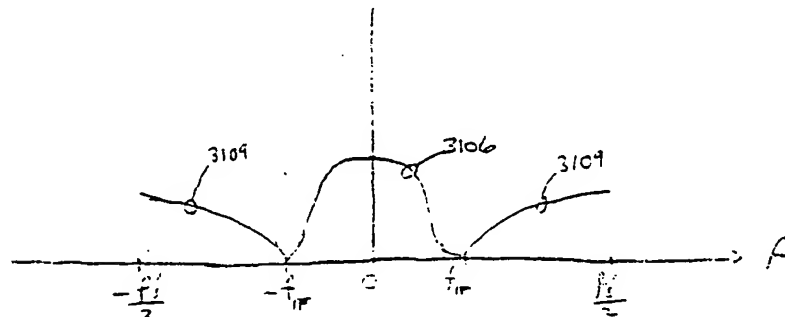
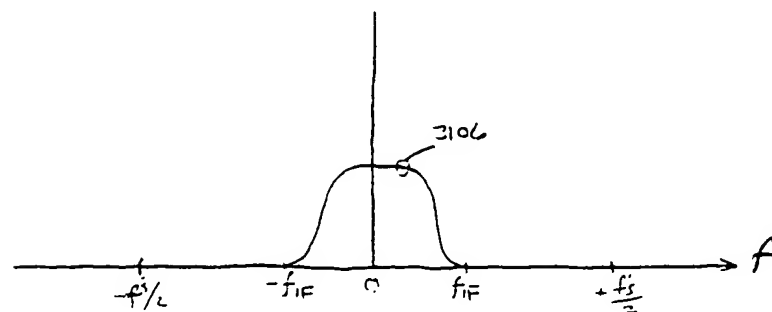


FIG. 35



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SECTION

FIG. 36A

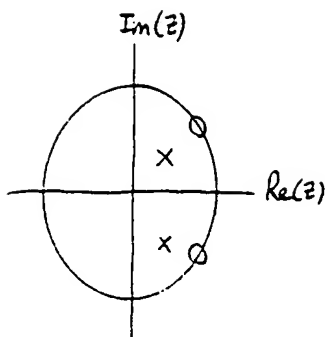


FIG. 36B

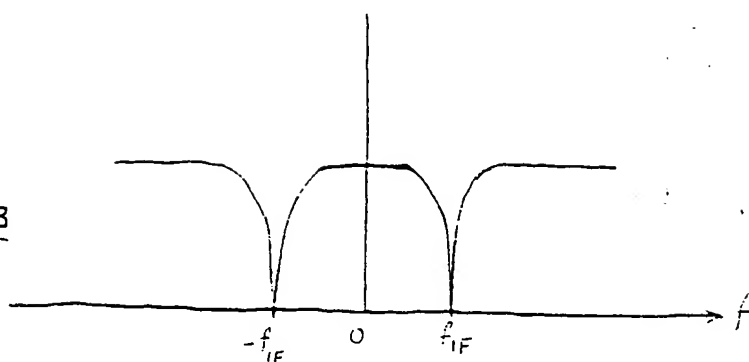


FIG. 37A

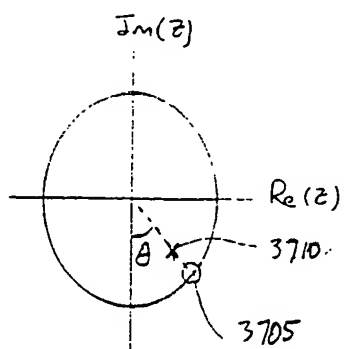
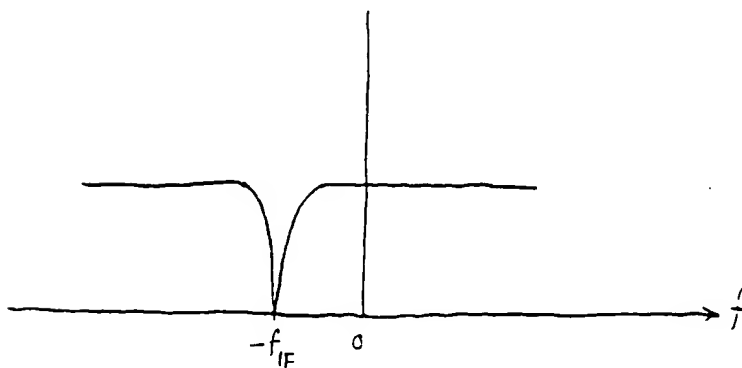
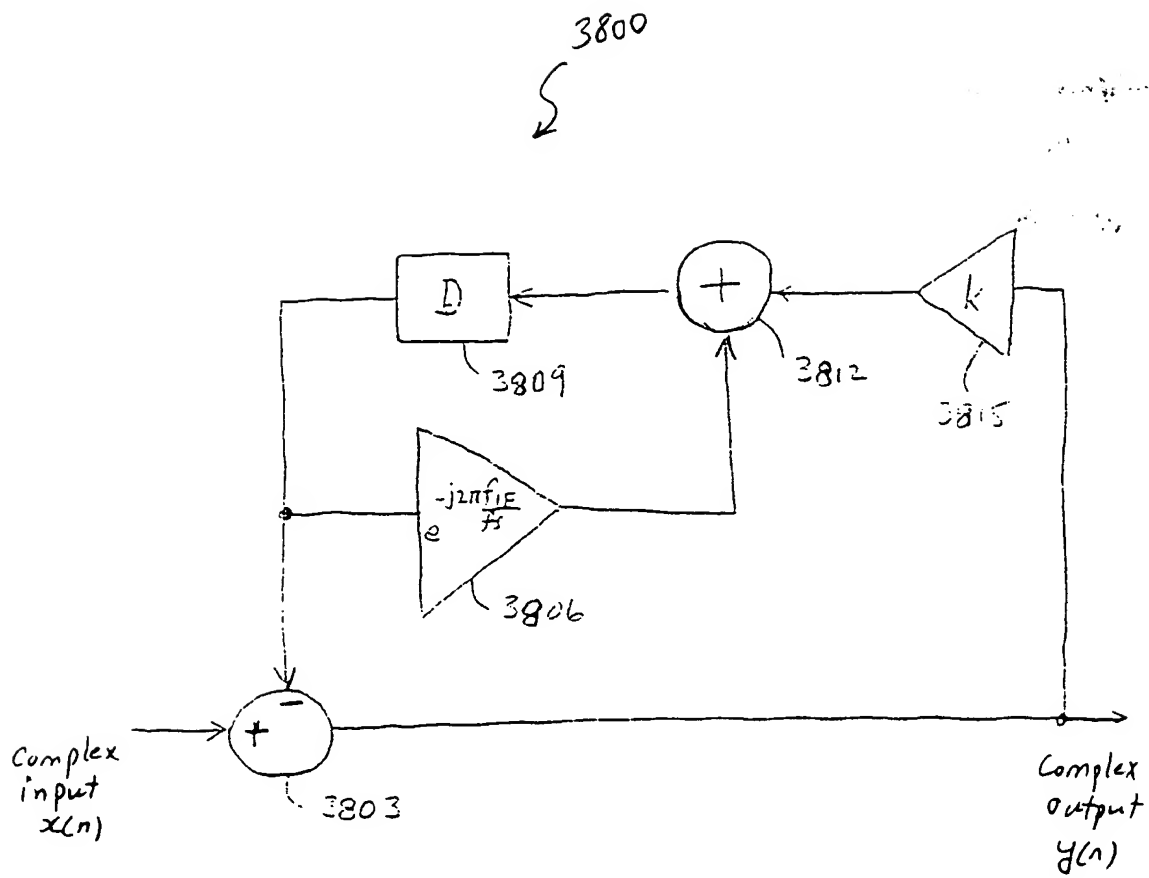


FIG. 37B



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U.S. PATENT & TRADEMARK OFFICE
MAR 19 1980

FIG. 38

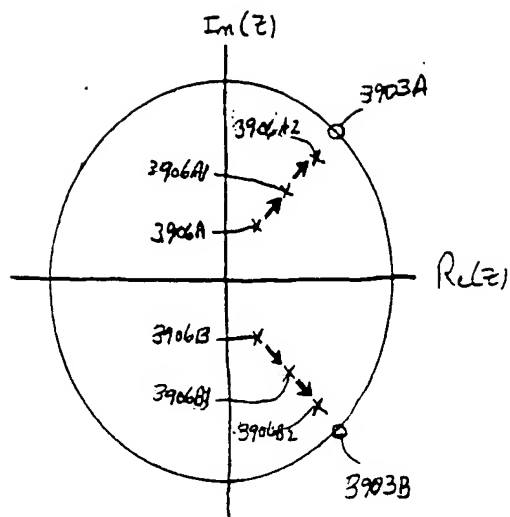


FIG. 39

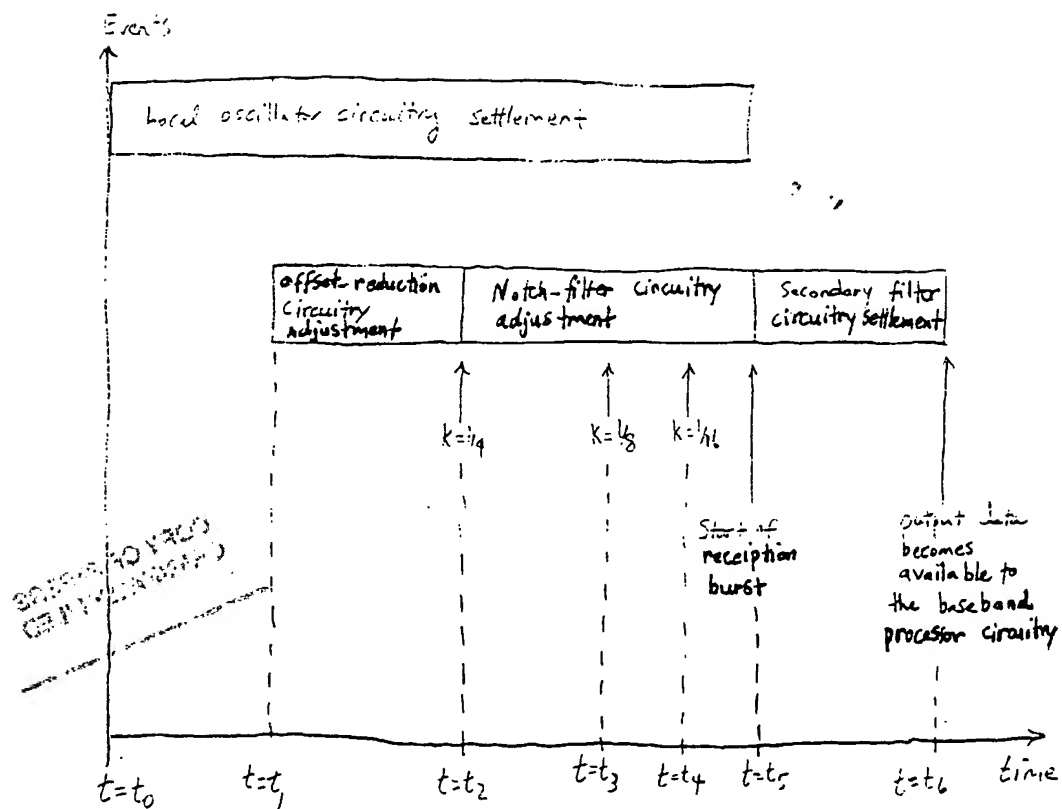


FIG. 40